ESP32-S3 Series SoC

Errata

Introduction

This document describes known errata in ESP32-S3 series of SoCs.

Version 1.2

Espressif Systems

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Contents

Chip Identification

> **Note:**
>
> Check the link or the QR code to make sure that you use the latest version of this document:
> https://espressif.com/documentation/esp32-s3_errata_en.pdf

1   Chip Revision

Espressif is introducing **vM.X** numbering scheme to indicate chip revisions.

M – Major number, indicating the major revision of the chip product. If this number changes, it means the software used for the previous version of the product is incompatible with the new product, and the software version shall be upgraded for the use of the new product.

X – Minor number, indicating the minor revision of the chip product. If this number changes, it means the software used for the previous version of the product is compatible with the new product, and there is no need to upgrade the software.

The vM.X scheme replaces previously used chip revision schemes, including ECOx numbers, Vxxx, and other formats if any.

The chip revision of ESP32-S3 is identified by:

- eFuse fields EFUSE_RD_MAC_SPI_SYS_5_REG[25:23] and EFUSE_RD_MAC_SPI_SYS_3_REG[20:18]

Table 1: Chip Revision Identification by eFuse Bits

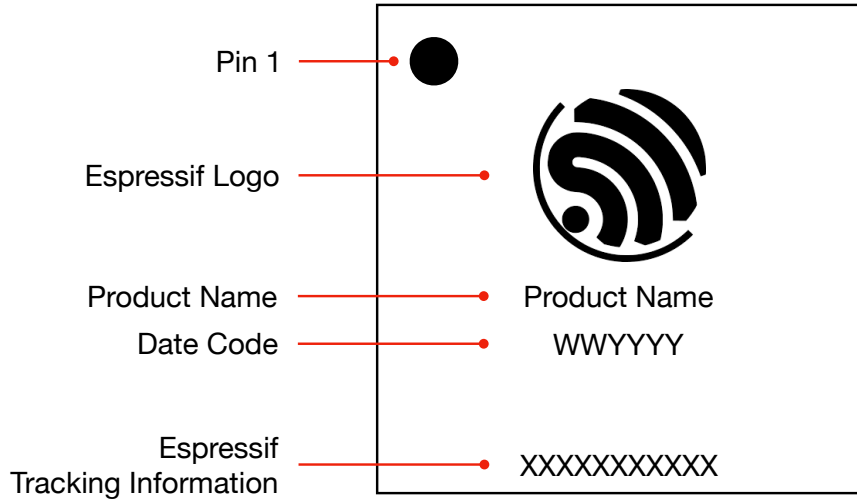|		Chip Revision		
	eFuse Bit	v0.0	v0.1	v0.2
Major Number	EFUSE_RD_MAC_SPI_SYS_5_REG[25]	0	0	0
	EFUSE_RD_MAC_SPI_SYS_5_REG[24]	0	0	0
Minor Number	EFUSE_RD_MAC_SPI_SYS_5_REG[23]	0	0	0
	EFUSE_RD_MAC_SPI_SYS_3_REG[20]	0	0	0
	EFUSE_RD_MAC_SPI_SYS_3_REG[19]	0	0	1
	EFUSE_RD_MAC_SPI_SYS_3_REG[18]	0	1	0

- **Espressif Tracking Information** line in chip marking

Figure 1: Chip Marking Diagram

Table 2: Chip Revision Identification by Chip Marking

Chip Revision	Espressif Tracking Information
v0.0	xAxxxxxx
v0.1	xBxxxxxx
v0.2	xCxxxxxx

- **Specification Identifier** line in module marking
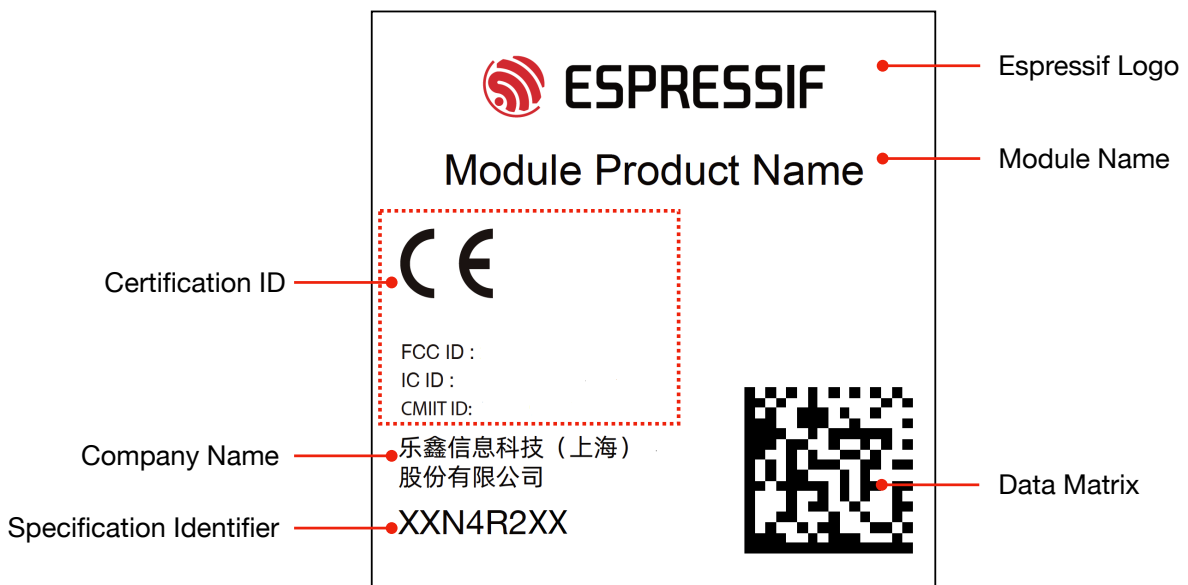

Figure 2: Module Marking Diagram

Table 3: Chip Revision Identification by Module Marking

Chip Revision	Specification Identifier[1]
v0.0	–
v0.1	M0XXXX
v0.2	MCXXXX

[1] – means modules with this chip revision are not mass produced.

> **Note:**
>
> - Information about ESP-IDF release that supports a specific chip revision is provided in Compatibility Between ESP-IDF Releases and Revisions of Espressif SoCs.
>
> - For more information about the chip revision upgrade and their identification of ESP32-S3 series products, please refer to ESP32-S3 Product/Process Change Notifications (PCN).
>
> - For more information about the chip revision numbering scheme, see Compatibility Advisory for Chip Revision Numbering Scheme.

2 Additional Methods

Some errors in the chip product don't need to be fixed at the silicon level, or in other words in a new chip revision.

In this case, the chip may be identified by **Date Code** in chip marking (see Figure 1). For more information, please refer to *Espressif Chip Packaging Information*.

Modules built around the chip may be identified by **PW Number** in product label (see Figure 3). For more information, please refer to *Espressif Module Packaging Information*.

Figure 3: Module Product Label

> **Note:**
> Please note that **PW Number** is only provided for reels packaged in aluminum moisture barrier bags (MBB).

Errata Description

<p align="center">**Table 4: Errata Summary**</p>

Category	Description	Affected Revisions[1]		
		v0.0	v0.1	v0.2
RTC	3.1 *RTC register read error after wake-up from Light-sleep mode*	Y	Y	Y
Analog Power	4.1 *Chip will be damaged when BIAS_SLEEP = 0 and PD_CUR = 1*	Y	Y	Y
LCD	5.1 *The LCD module exhibits unreliable behavior when certain clock dividers are used*	Y	Y	Y
USB-OTG	6.1 *The USB-OTG Download function is unavailable*	Y	Y	Y*
RMT	7.1 *The idle state signal level might run into error in RMT continuous TX mode*	Y	Y	Y
Touch Sensor	8.1 *The TOUCH_SCAN_DONE_INT interrupt raw data value is undefined*	Y	Y	Y
SAR ADC	9.1 *The digital controller (DMA) of SAR ADC2 cannot work*	Y	Y	Y

[1] Y* means some batches of a revision are affected.

3   RTC

3.1   RTC register read error after wake-up from Light-sleep mode

Description

If an RTC peripheral is turned off in Light-sleep mode, there is a certain probability that after waking up from Light-sleep, the CPU of ESP32-S3 will read the registers in the RTC power domain incorrectly.

Workarounds

Users are suggested not to power down RTC peripherals in Light-sleep mode. There will be no impact on power consumption.

This issue has been bypassed in ESP-IDF v4.4 and above.

Projected Solution

No fix scheduled.

4   Analog Power

4.1   Chip will be damaged when BIAS_SLEEP = 0 and PD_CUR = 1

Description

If the analog power is configured as BIAS_SLEEP = 0 and PD_CUR = 1, the chip will be permanently damaged. This issue might be triggered when ULP and/or touch sensor is used during Light-sleep or Deep-sleep.

Workarounds

Users are suggested to disable such analog power configuration in sleep mode through software.

This issue has been bypassed by disabling the above configuration in ESP-IDF v4.4.2+, v5.0 and above.

Projected Solution

No fix scheduled.

5   LCD

5.1   The LCD module exhibits unreliable behavior when certain clock dividers are used

Description

1. When the RGB format is used, if the clock divider is set to 1, i.e., LCD_CAM_LCD_CLK_EQU_SYSCLK = 1:

    - The pixel clock output (LCD_PCLK) will not be able to be set to falling edge trigger.

    - When frames are continuously sent in this mode (i.e., LCD_CAM_LCD_NEXT_FRAME_EN = 1), it might occur that the second frame inserts the last data of the previous frame in the first frame.

2. When the I8080 format is used, if the clock cycle of the LCD core clock (LCD_CLK) before data transmission is less than or equal to 2, it can result in incorrect value of the first data and the subsequent data quantity.

Note:

Please refer to the following steps to obtain the clock cycle before data transmission with the I8080 format.

The clock cycle before data transmission depends on the following factors:

- VFK cycle length (unit: LCD_PCLK): The clock cycle length during the VFK phase

- CMD cycle length (unit: LCD_PCLK): The clock cycle length during the CMD phase

- DUMMY cycle length (unit: LCD_PCLK): The clock cycle length during the DUMMY phase

- LCD_CAM_LCD_CLK_EQU_SYSCLK: Decides if LCD_PCLK equals LCD_CLK

- LCD_CAM_LCD_CLKCNT_N: Decides the division relationship between LCD_PCLK and LCD_CLK

Based on the information above, three variables are defined below:

- **total_pixel** = VFK cycle length + CMD cycle length + DUMMY cycle length
- **cycle_unit** =
    - 1, if LCD_CAM_LCD_CLK_EQU_SYSCLK = 1
    - LCD_CAM_LCD_CLKCNT_N + 1, if LCD_CAM_LCD_CLK_EQU_SYSCLK = 0

> • ahead_cycle = **total_pixel** * **cycle_unit**
>
> **ahead_cycle** indicates the clock cycle before data transmission, which, if less than or equal to 2, will cause an error.

Workarounds

Users are suggested to do the followings:

- When using the RGB format, avoid configuring LCD_CAM_LCD_CLK_EQU_SYSCLK as 1.

- When using the I8080 format:

    - try to avoid configuring LCD_CAM_LCD_CLK_EQU_SYSCLK as 1.

    - ensure that **ahead_cycle** is larger than 2 if LCD_CAM_LCD_CLK_EQU_SYSCLK has to be set as 1.

This issue has been bypassed through the methods described above in ESP-IDF v4.4.5+, v5.0.3+, v5.1 and above.

Projected Solution

No fix scheduled.

6   USB-OTG

6.1   The USB-OTG Download function is unavailable

Description

For ESP32-S3 series chips manufactured before the Date Code 2219 and ESP32-S3 series of modules and development boards with the PW Number before PW-2022-06-XXXX, the EFUSE_DIS_USB_OTG_DOWNLOAD_MODE (BLK0 B19[7]) bit of eFuse is set by default and cannot be modified. Therefore, the USB-OTG Download function is unavailable for these products.

> **Note:**
> For detailed information about the Date Code and the PW Number, please refer to 2 *Additional Methods.*

Workarounds

ESP32-S3 also supports downloading firmware through USB-Serial-JTAG. Please refer to USB Serial/JTAG Controller Console.

Projected Solution

This issue has been fixed.

For ESP32-S3 series chips manufactured on and after the Date Code 2219 and ESP32-S3 series modules and development boards with the PW Number of and after PW-2022-06-XXXX, the bit (BLK0 B19[7]) will not be programmed by default and thus is open for users to program. This will enable the USB-OTG Download function.

For more details and recommendations for users, please refer to Security Advisory for USB_OTG & USB_Serial_JTAG Download Functions of ESP32-S3 Series Products.

7 RMT

7.1 The idle state signal level might run into error in RMT continuous TX mode

Description

In ESP32-S3's RMT module, if the continuous TX mode is enabled, it is expected that the data transmission stops after the data is sent for RMT_TX_LOOP_NUM_CHn rounds, and after that, the signal level in idle state should be controlled by the "level" field of the end-marker.

However, in real situation, after the data transmission stops, the channel's idle state signal level is not controlled by the "level" field of the end-marker, but by the level in the data wrapped back, which is indeterminate.

Workarounds

Users are suggested to set RMT_IDLE_OUT_EN_CHn to 1 to only use registers to control the idle level.

This issue has been bypassed since the first ESP-IDF version that supports continuous TX mode (v5.0). In these versions of ESP-IDF, it is configured that the idle level can only be controlled by registers.

Projected Solution

No fix scheduled.

8 Touch Sensor

8.1 The TOUCH_SCAN_DONE_INT interrupt raw data value is undefined

Description

For ESP32-S3's touch sensor, the raw data value is undefined for the first two TOUCH_SCAN_DONE_INT interrupts.

Workarounds

Users are suggested to skip the first two TOUCH_SCAN_DONE_INT interrupts, then turn them off and stop using them.

Projected Solution

No fix scheduled.

9 SAR ADC

9.1 The digital controller (DMA) of SAR ADC2 cannot work

Description

The digital controller of SAR ADC2, i.e., DIG ADC2 controller, may receive a false sampling enable signal. In such case, the controller will enter an inoperative state.

Workarounds

No workaround. Users are suggested to use RTC controller to control SAR ADC2.

Projected Solution

No fix scheduled.

Related Documentation and Resources

Related Documentation

- ESP32-S3 Series Datasheet – Specifications of the ESP32-S3 hardware.
- ESP32-S3 Technical Reference Manual – Detailed information on how to use the ESP32-S3 memory and peripherals.
- ESP32-S3 Hardware Design Guidelines – Guidelines on how to integrate the ESP32-S3 into your hardware product.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32-S3 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns?keys=ESP32-S3
- *ESP32-S3 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories?keys=ESP32-S3
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32-S3 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-S3 Series SoCs* – Browse through all ESP32-S3 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-S3
- *ESP32-S3 Series Modules* – Browse through all ESP32-S3-based modules.
  https://espressif.com/en/products/modules?id=ESP32-S3
- *ESP32-S3 Series DevKits* – Browse through all ESP32-S3-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32-S3
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

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  https://espressif.com/en/contact-us/sales-questions

Revision History

Date	Version	Release Notes
2023-11-15	v1.2	• Adjusted the section order in *Errata Description* and added the following sections: – Section 3.1 *RTC register read error after wake-up from Light-sleep mode* – Section 5.1 *The LCD module exhibits unreliable behavior when certain clock dividers are used* – Section 7.1 *The idle state signal level might run into error in RMT continuous TX mode* – Section 8.1 *The TOUCH_SCAN_DONE_INT interrupt raw data value is undefined* • Added information about how to identify chip revisions in modules in Section 1 *Chip Revision* • Added Section 2 *Additional Methods* • Added a note under Table 4 • Other minor updates
2023-01-20	v1.1	Added Section 6
2022-10-14	v1.0	First release