ESPRESSIF

-
-

-
-

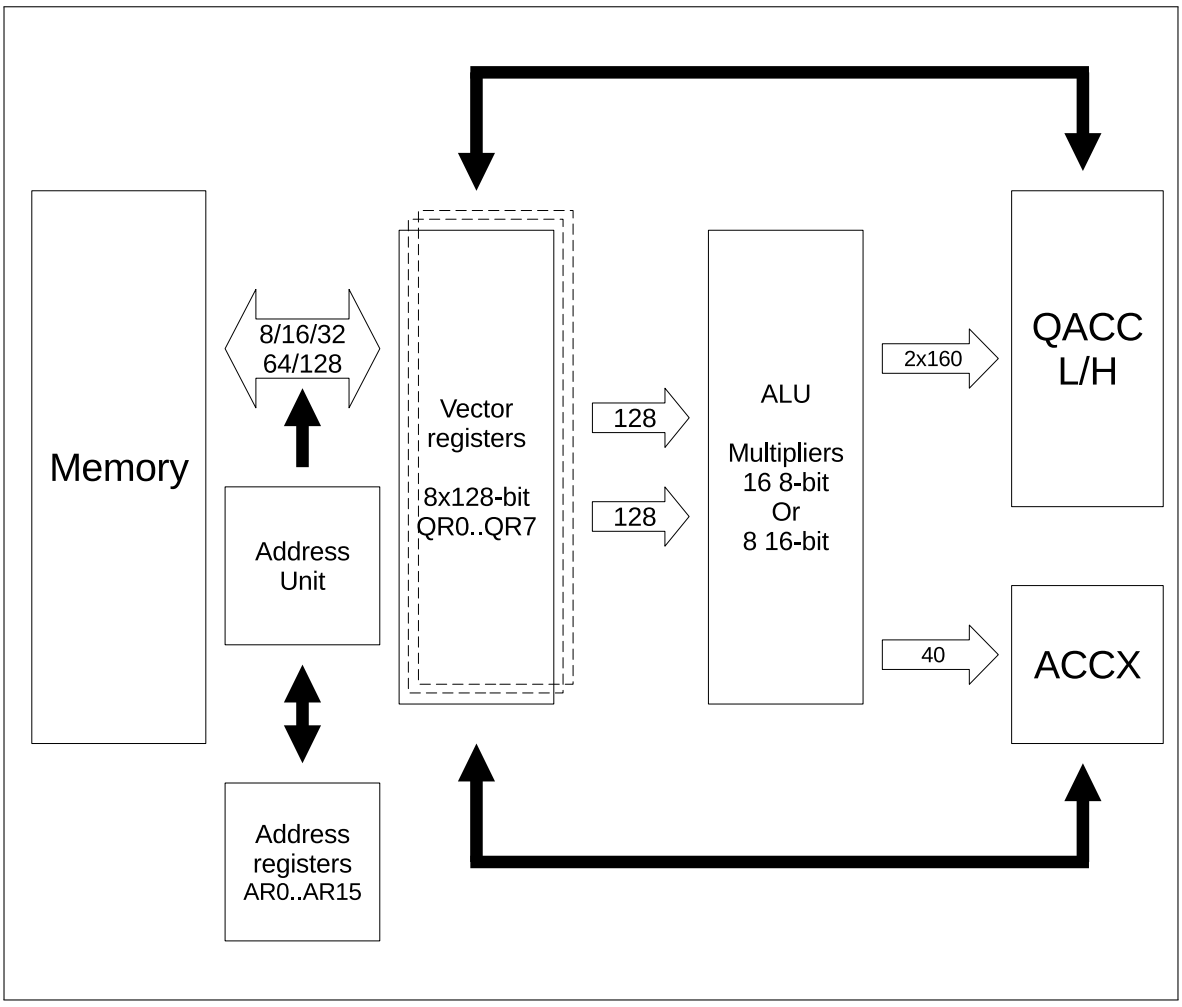
$R/\overline{W}$

μ

μ

$KeyKey_AKey_BKey_C$

-
-
-
-
-


Memory
8/16/32
64/128
Address
Unit
Address
registers
AR0..AR15
Vector
registers
8x128-bit
QR0..QR7
128
128
ALU
Multipliers
16 8-bit
Or
8 16-bit
2x160
40
QACC
L/H
ACCX

-
-
-

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-

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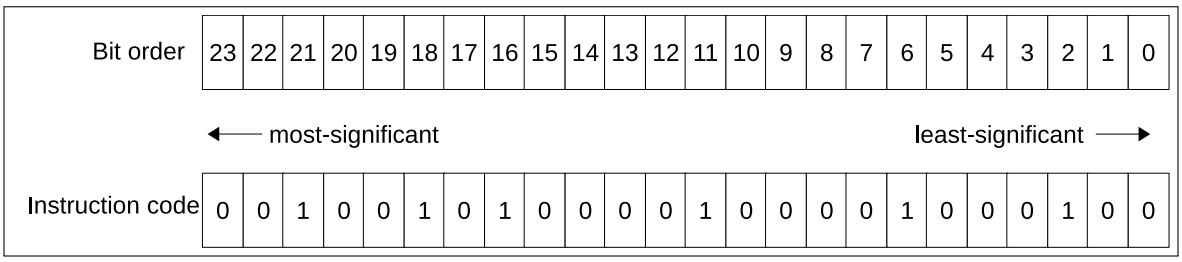
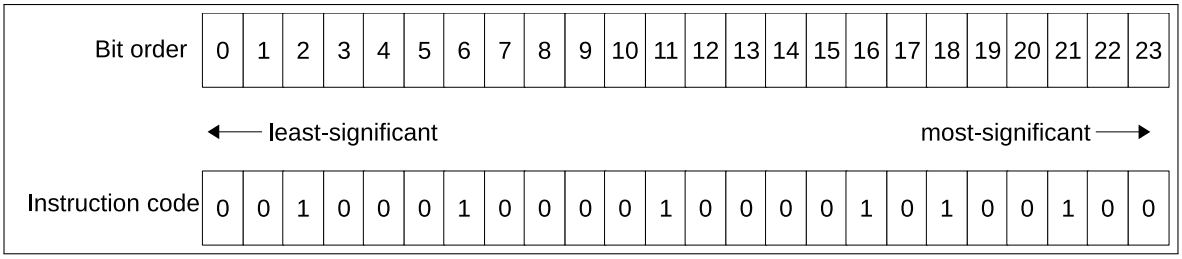
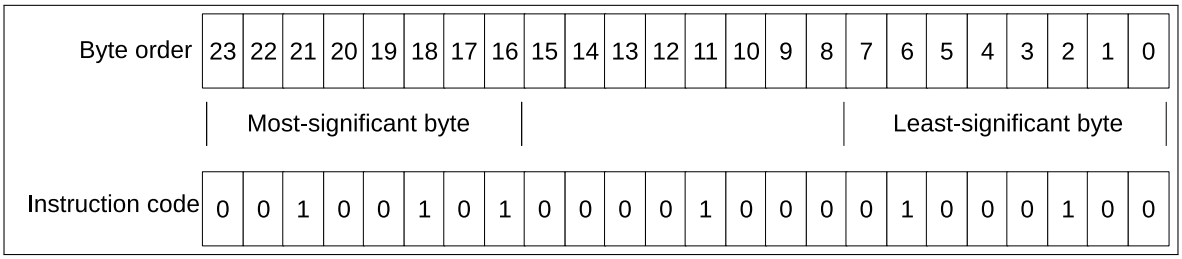
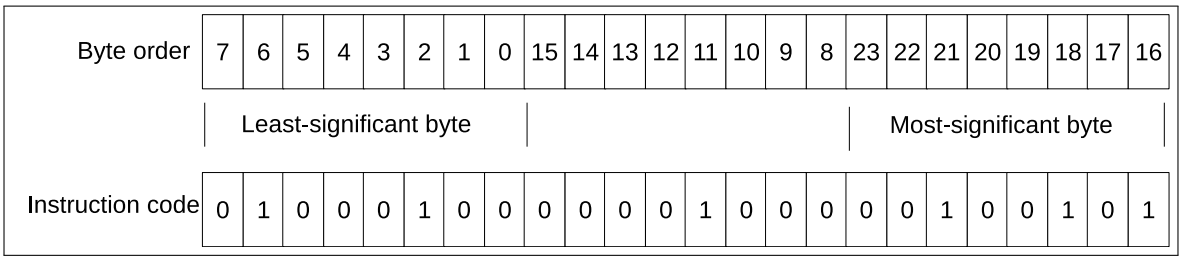
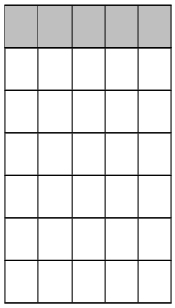
-
-


Bit order
23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
most-significant
least-significant
Instruction code
0 0 1 0 0 1 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 1 0 0


Bit order
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
least-significant
most-significant
Instruction code
0 0 1 0 0 0 1 0 0 0 0 1 0 0 0 0 1 0 1 0 0 1 0 0

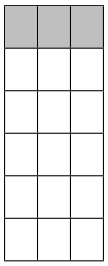

Byte order
23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Most-significant byte
Least-significant byte
Instruction code
0 0 1 0 0 1 0 1 0 0 0 0 1 0 0 0 0 1 0 0 0 1 0 0


Byte order
7 6 5 4 3 2 1 0 15 14 13 12 11 10 9 8 23 22 21 20 19 18 17 16
Least-significant byte
Most-significant byte
Instruction code
0 1 0 0 0 1 0 0 0 0 0 0 1 0 0 0 0 0 1 0 0 1 0 1



$EE.VADDS.S8q2, q0, q1$

$EE.VMUL.S16q2, q0, q1$



aligned(16)

EE.LD.128.*USAR.IP* $q0$, $a8$, 16
EE.VLD.128.*IP* $q1$, $a8$, 16
EE.SRC.Q $q2$, $q0$, $q1$

	$qa = qx \vert qy$
	$qa = qxqy$
	$qa = qxqy$
	$qa = qx$

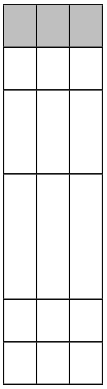
*

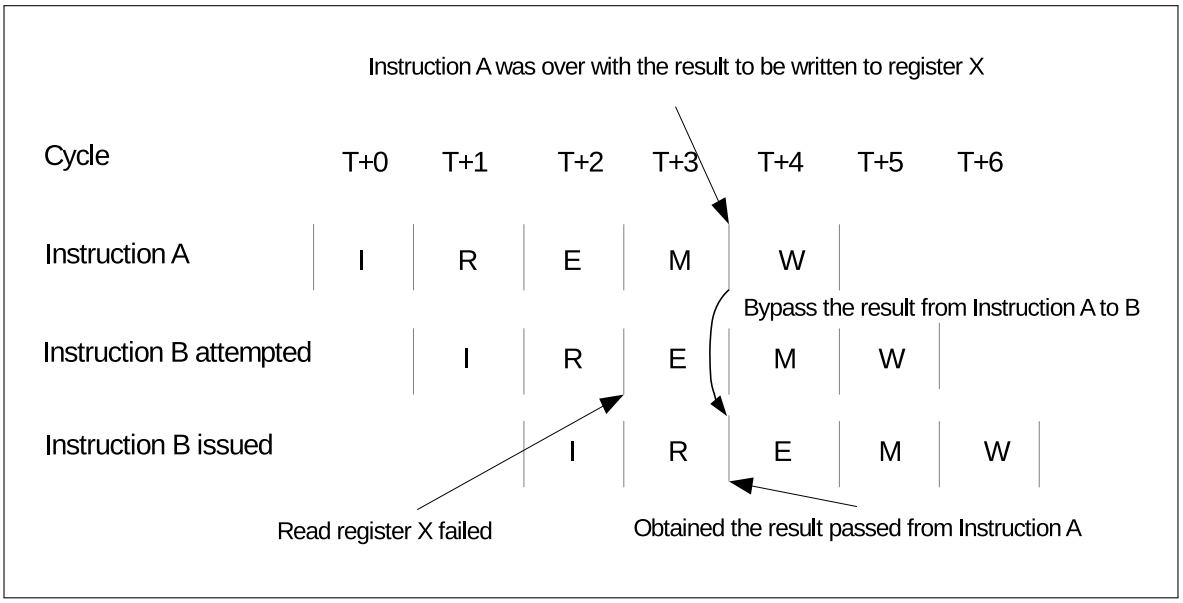
*

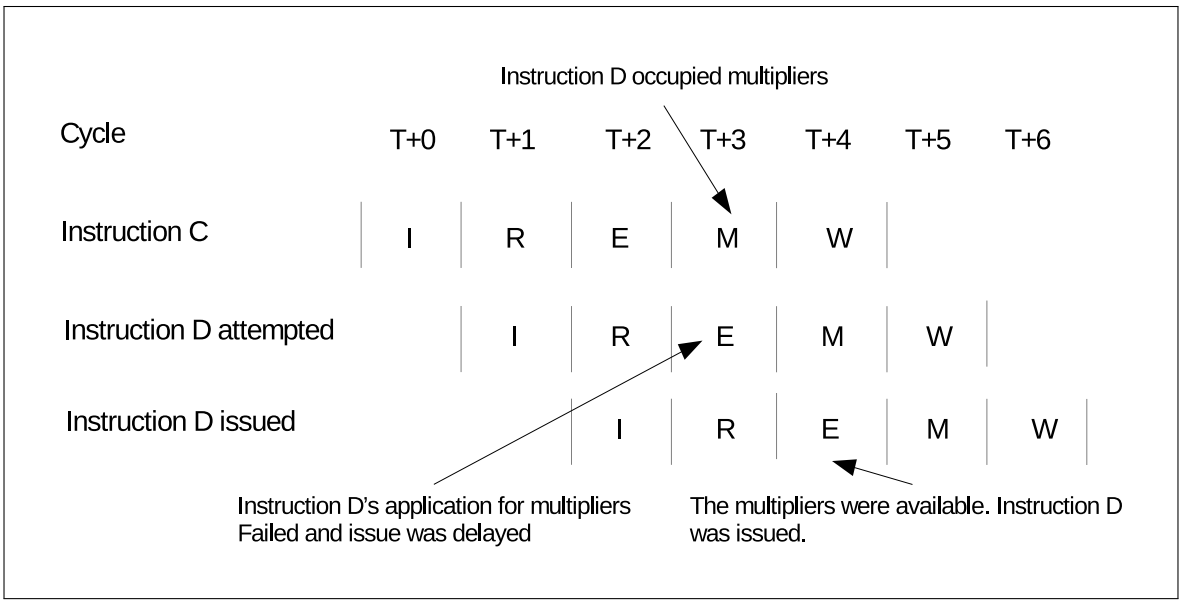
*

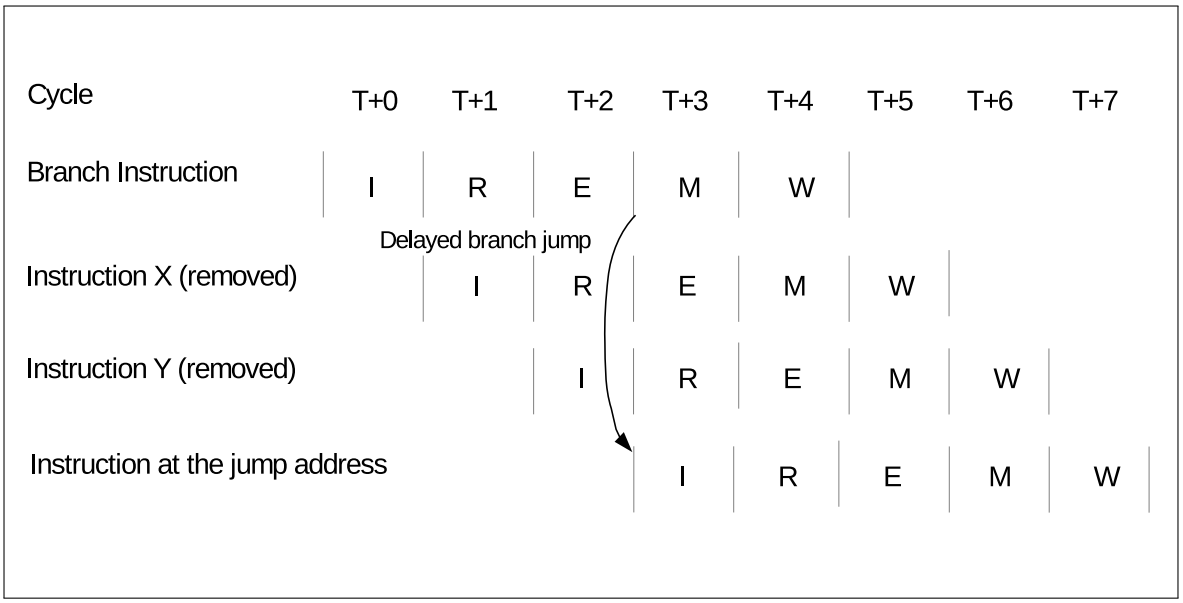
*

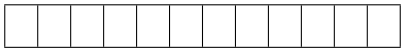
*

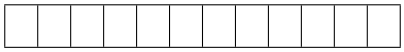


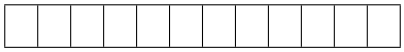

Instruction A was over with the result to be written to register X
Cycle
T+0
T+1
T+2
T+3
T+4
T+5
T+6
Instruction A
I
R
E
M
W
Bypass the result from Instruction A to B
Instruction B attempted
I
R
E
M
W
Instruction B issued
I
R
E
M
W
Read register X failed
Obtained the result passed from Instruction A

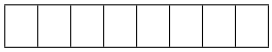

Instruction D occupied multipliers
Cycle
T+0
T+1
T+2
T+3
T+4
T+5
T+6
Instruction C
I
R
E
M
W
Instruction D attempted
I
R
E
M
W
Instruction D issued
I
R
E
M
W
Instruction D's application for multipliers Failed and issue was delayed
The multipliers were available. Instruction D was issued.

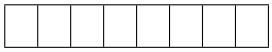

Cycle
T+0
T+1
T+2
T+3
T+4
T+5
T+6
T+7
Branch Instruction
I
R
E
M
W
Delayed branch jump
Instruction X (removed)
I
R
E
M
W
Instruction Y (removed)
I
R
E
M
W
Instruction at the jump address
I
R
E
M
W

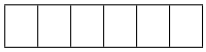


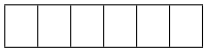


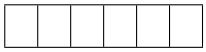


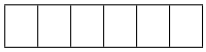


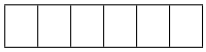


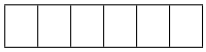


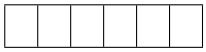


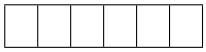


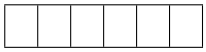


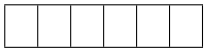


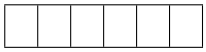


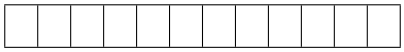


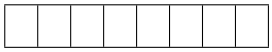


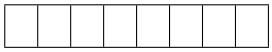


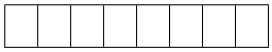


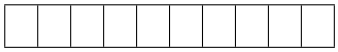


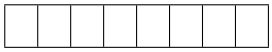


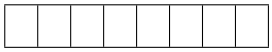


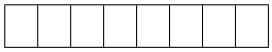


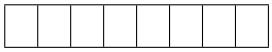


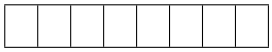


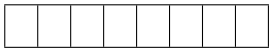


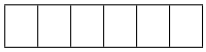


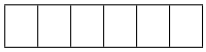


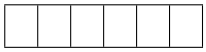


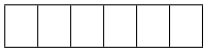


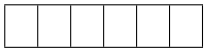


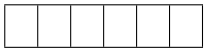


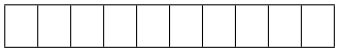


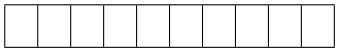


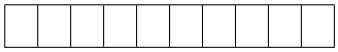


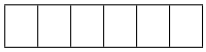


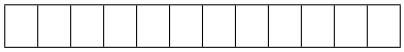


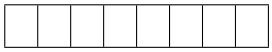


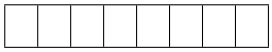


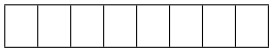


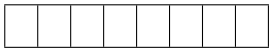


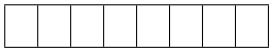


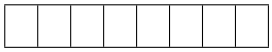


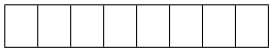


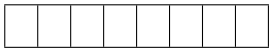


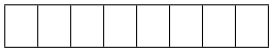


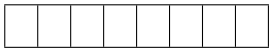


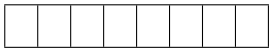


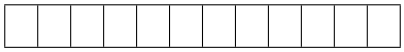


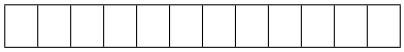


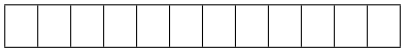


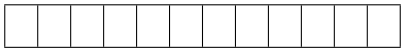


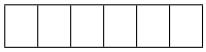


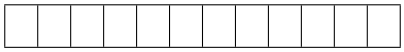


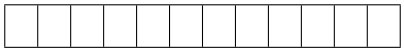


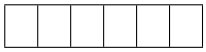


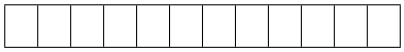


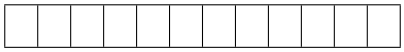


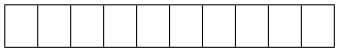


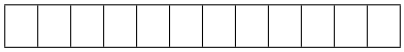


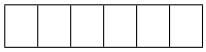


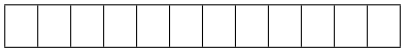


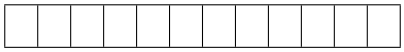


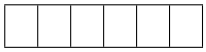


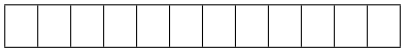


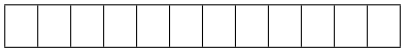


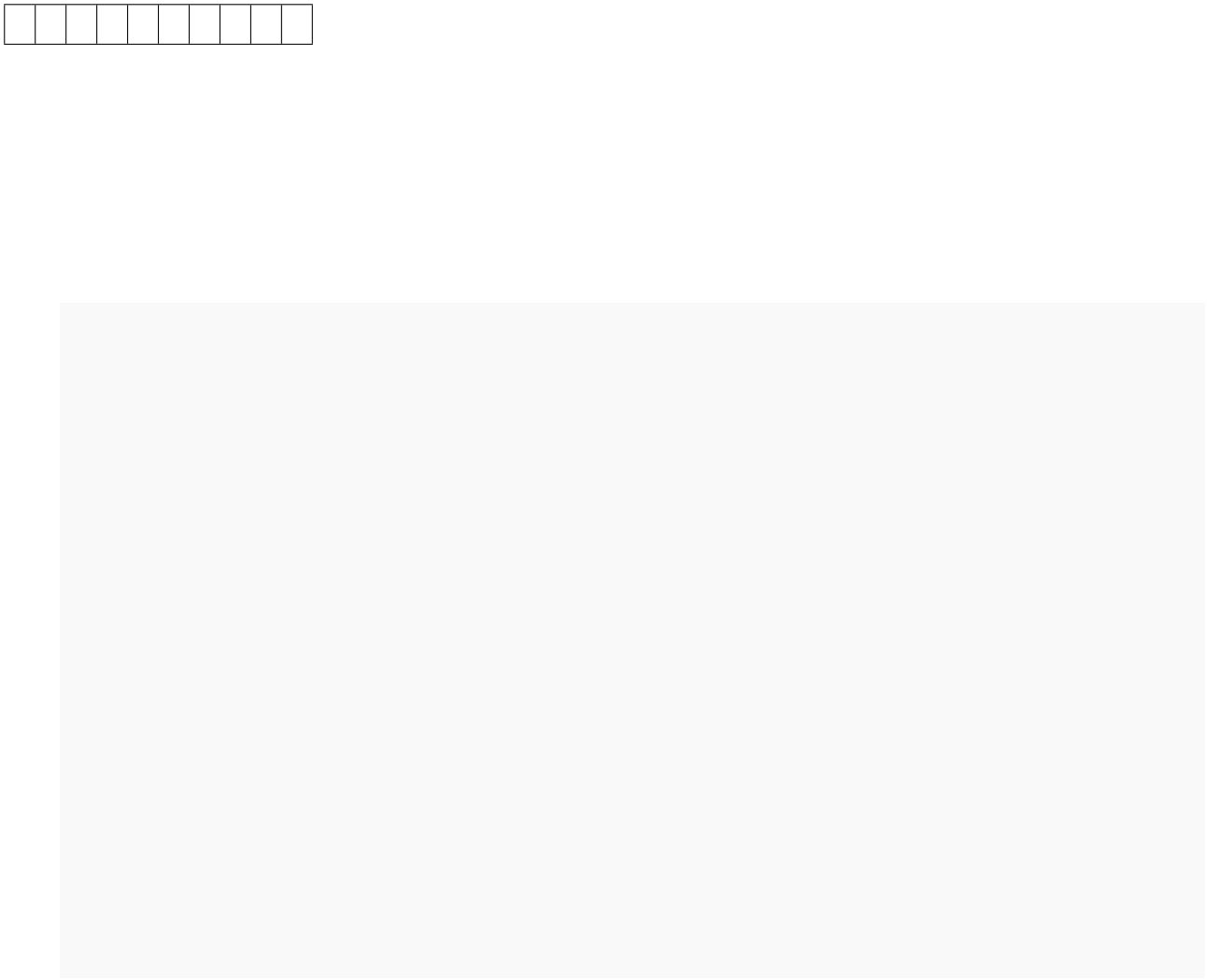


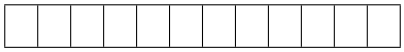


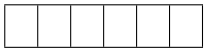


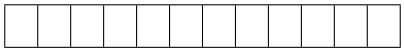


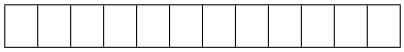


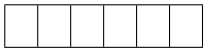


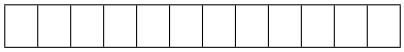


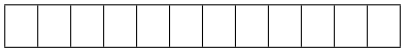


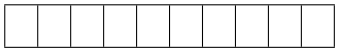


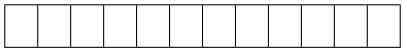


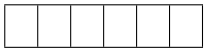


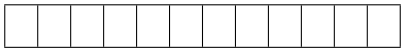


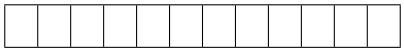


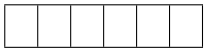


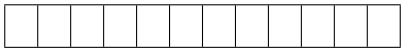


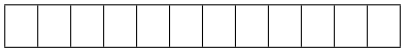


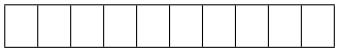


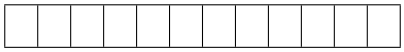


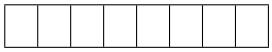


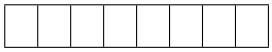


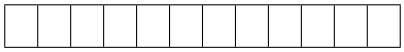


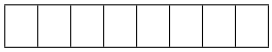


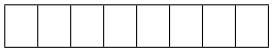


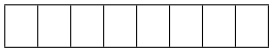


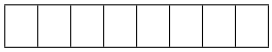


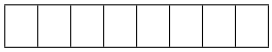


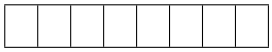


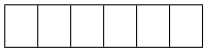


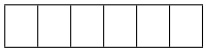


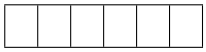


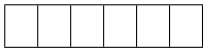


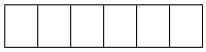


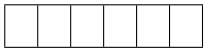


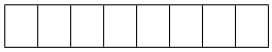


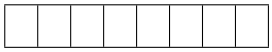


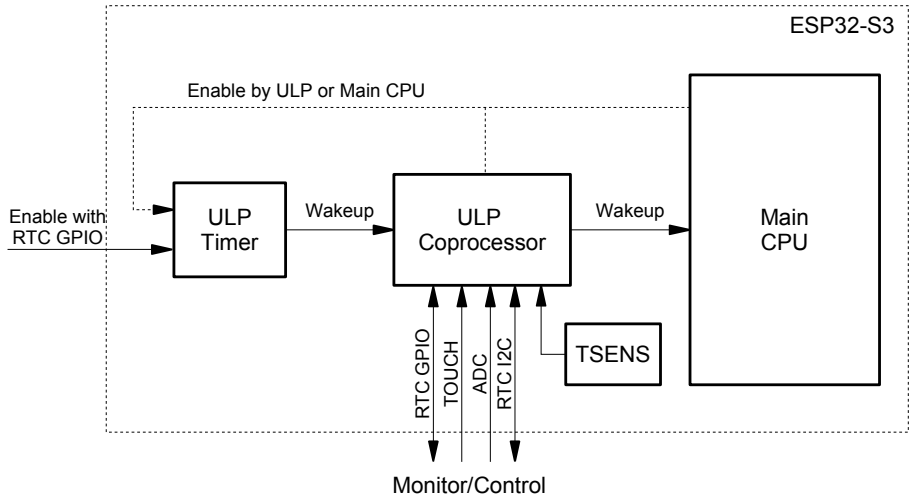











ESP32-S3
Enable by ULP or Main CPU
Enable with
RTC GPIO
ULP
Timer
Wakeup
ULP
Coprocessor
Wakeup
Main
CPU
TSENS
RTC GPIO
TOUCH
ADC
RTC I2C
Monitor/Control

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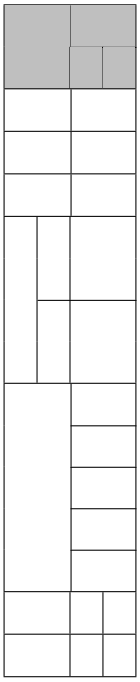
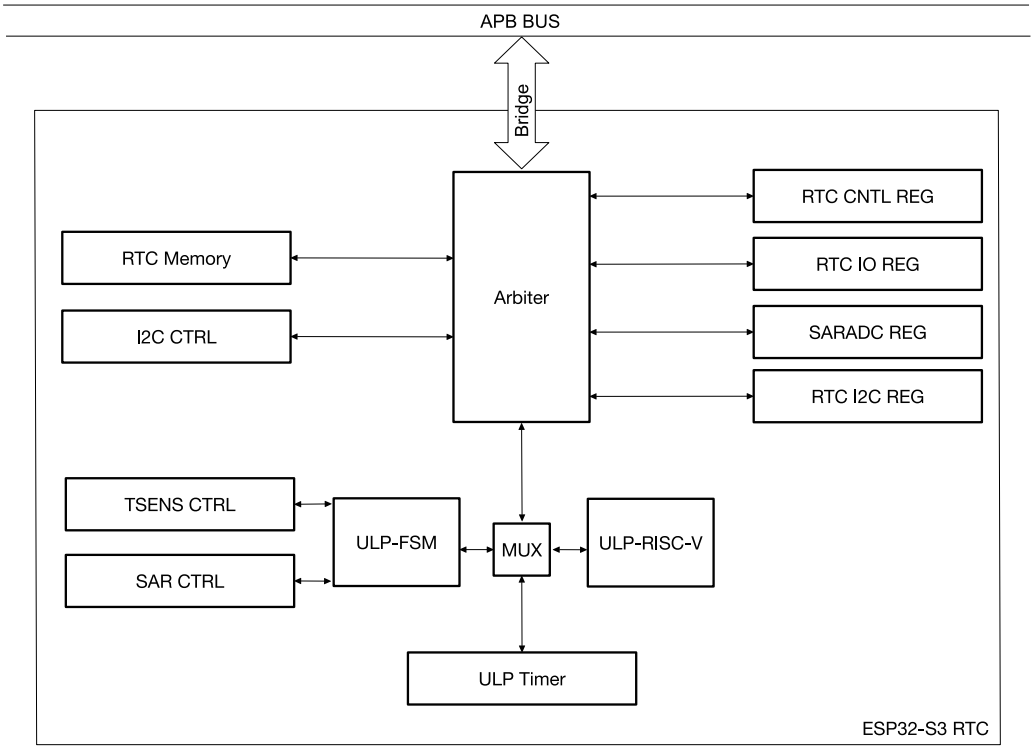
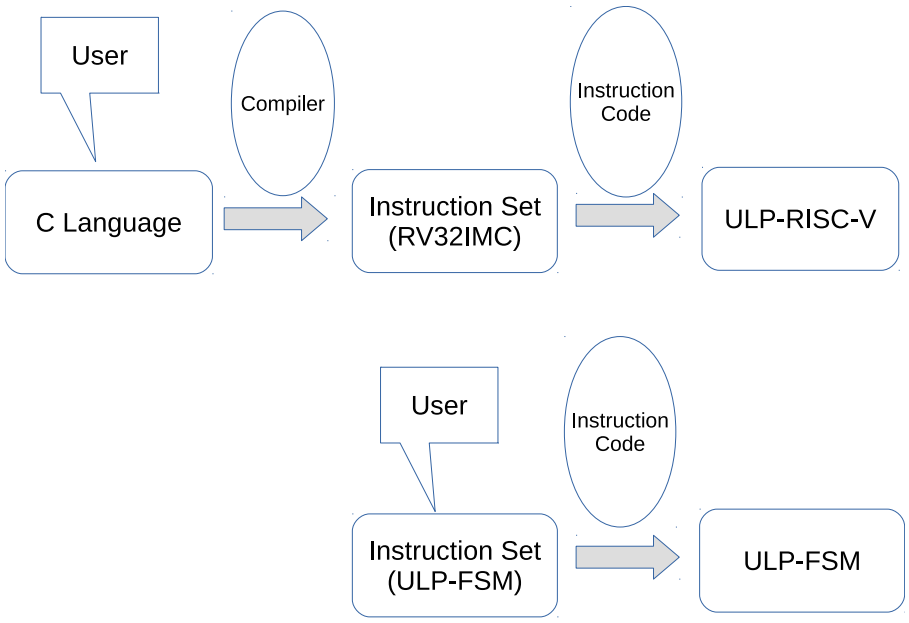
-




APB BUS
Bridge
RTC Memory
I2C CTRL
Arbiter
RTC CNTL REG
RTC IO REG
SARADC REG
RTC I2C REG
TSENS CTRL
SAR CTRL
ULP-FSM
MUX
ULP-RISC-V
ULP Timer
ESP32-S3 RTC


User
C Language
Compiler
Instruction Set
(RV32IMC)
Instruction
Code
ULP-RISC-V
User
Instruction Set
(ULP-FSM)
Instruction
Code
ULP-FSM

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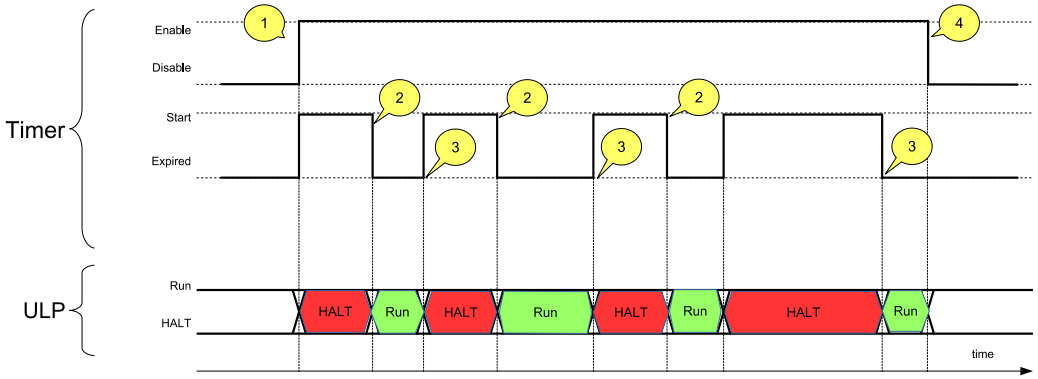
Timer
Enable
Disable
Start
Expired
1
2
3
4
ULP
Run
HALT
time

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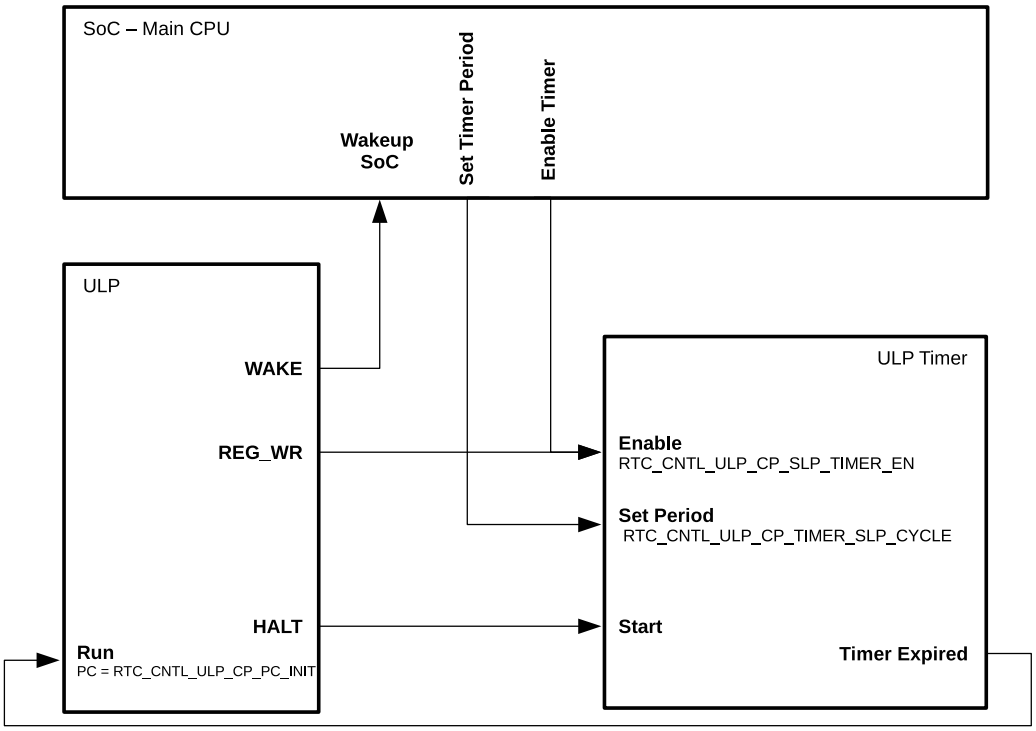
SoC – Main CPU
Wakeup SoC
Set Timer Period
Enable Timer
ULP
WAKE
REG_WR
HALT
Run
PC = RTC_CNTL_ULP_CP_PC_INIT
ULP Timer
Enable
RTC_CNTL_ULP_CP_SLP_TIMER_EN
Set Period
RTC_CNTL_ULP_CP_TIMER_SLP_CYCLE
Start
Timer Expired

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31 28	27 0

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31 28	27 26	25	24 21	20 6	5 4	3 2	1 0

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31 28	27 26	25	24 21	20	19 4	3 2	1 0

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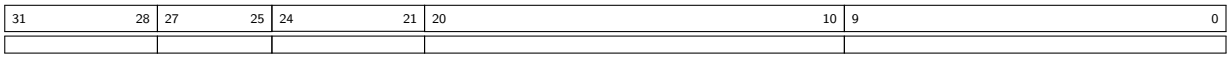
31 28	27	26	25	24 21	20 10	9	8 7	6	5 4	3 2	1 0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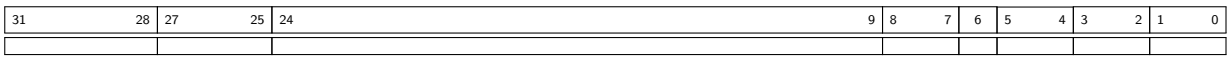
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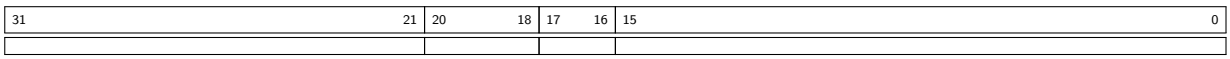
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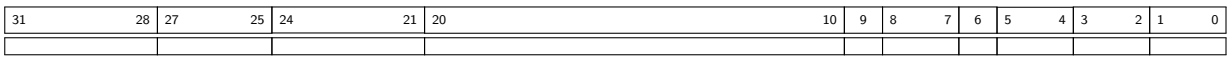
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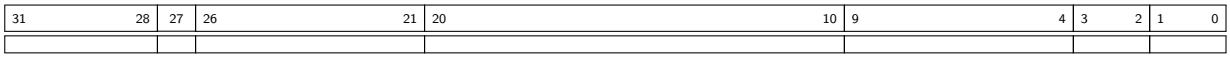
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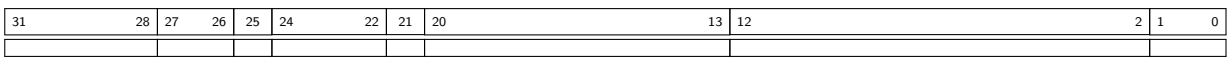
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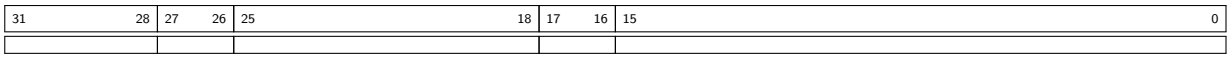
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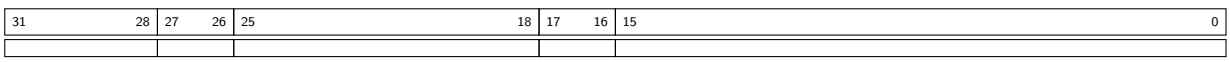
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31 28	27 16	15 2	1 0

31 28	27 7	6	5 2	1 0

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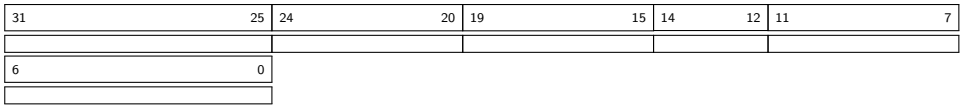
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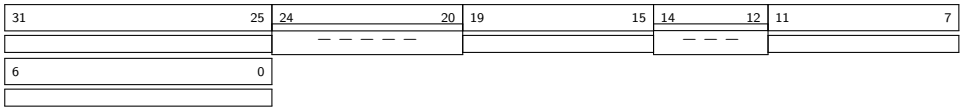
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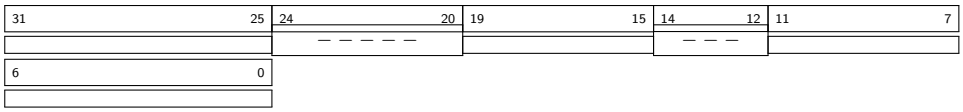
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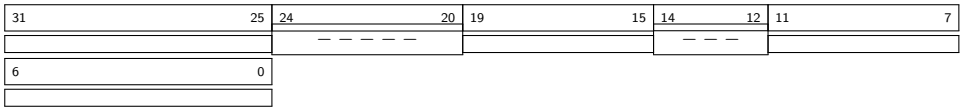
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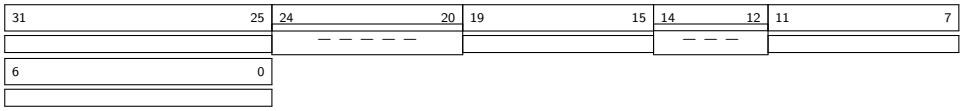
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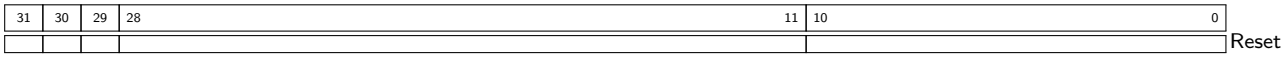
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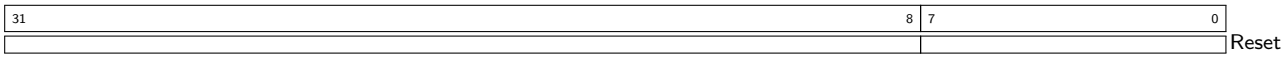
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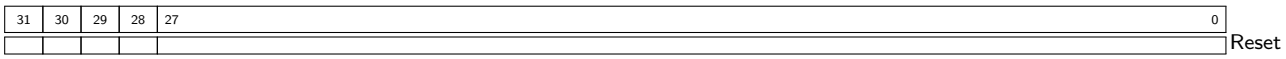
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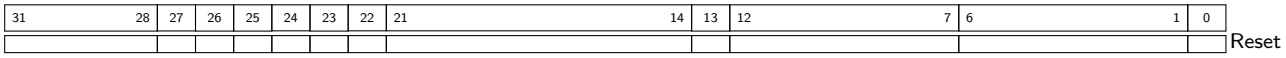
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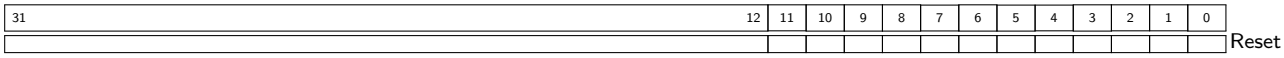
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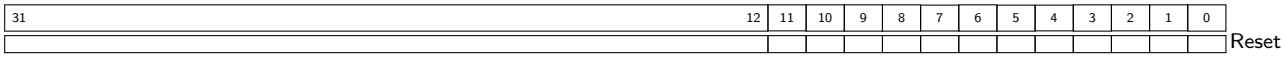
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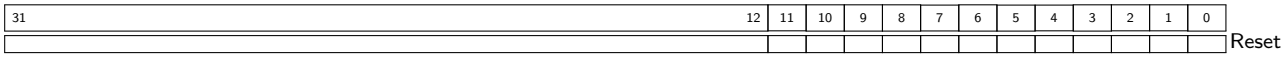
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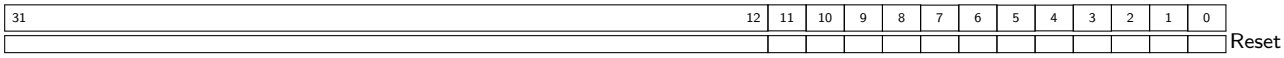
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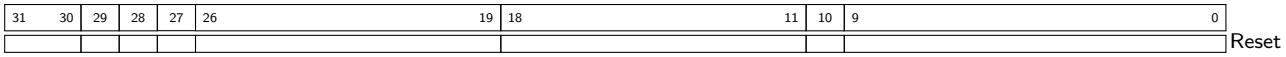
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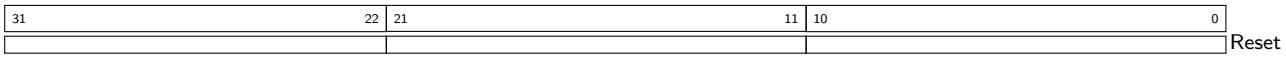
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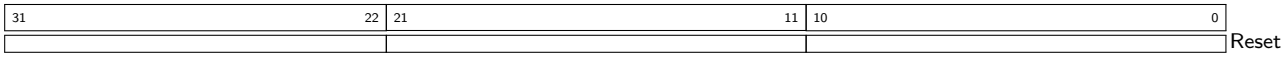
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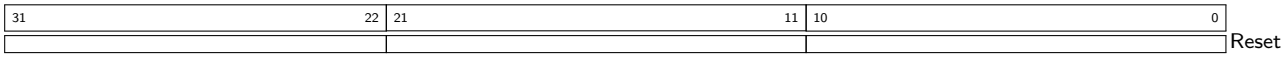
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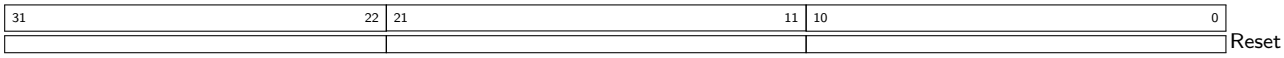
Reset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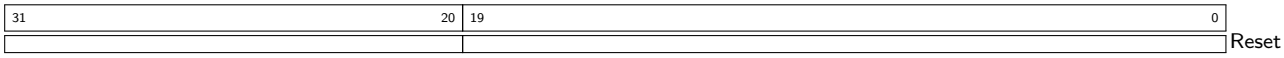
Reset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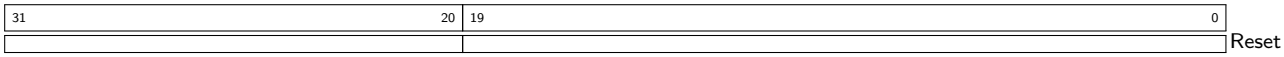
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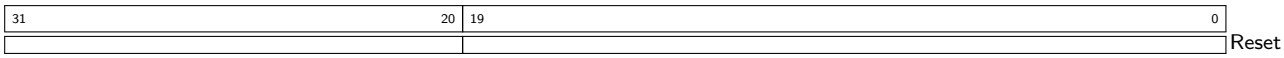
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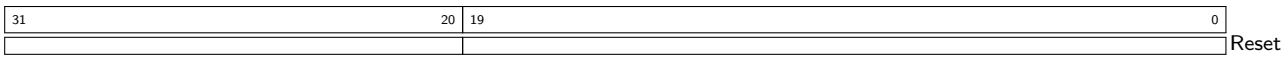
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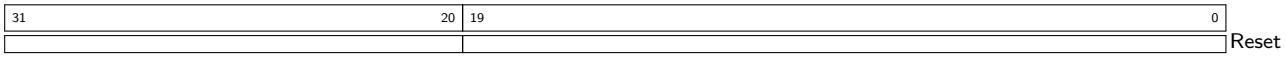
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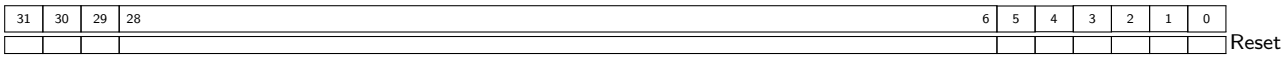
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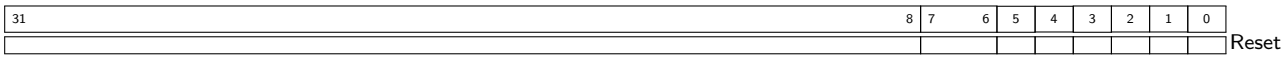
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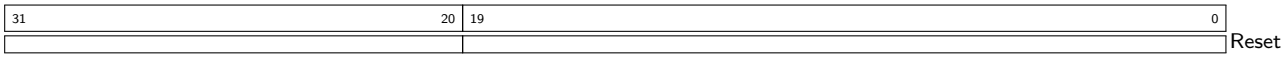
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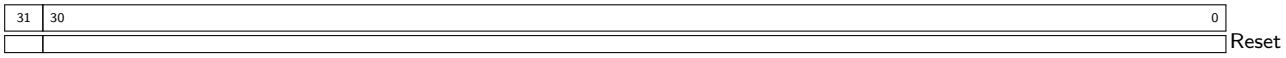
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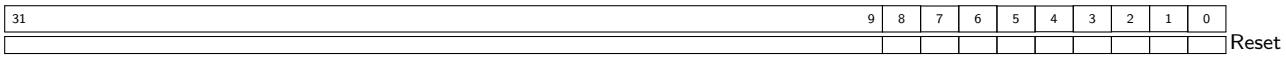
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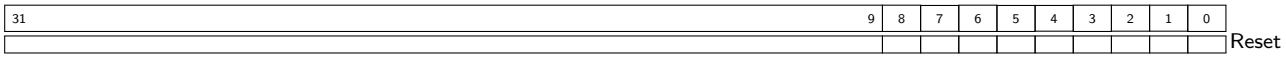
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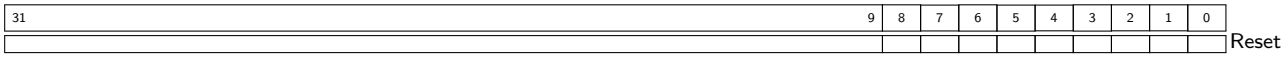
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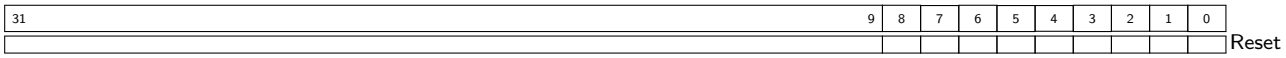
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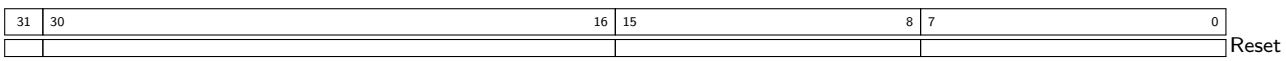
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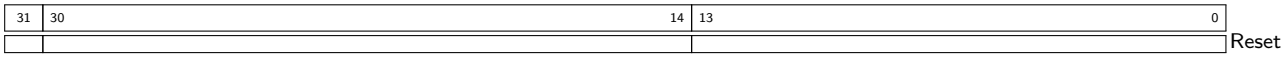
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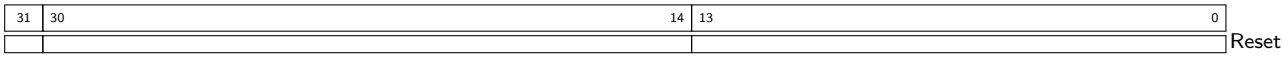
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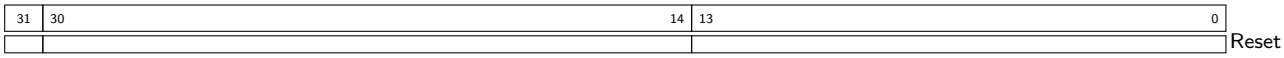
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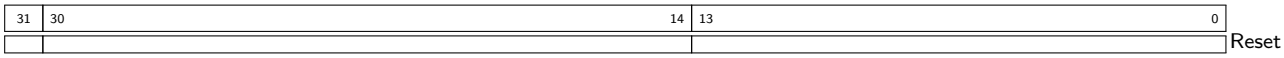
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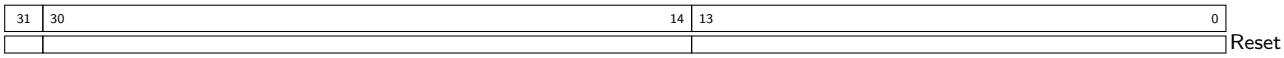
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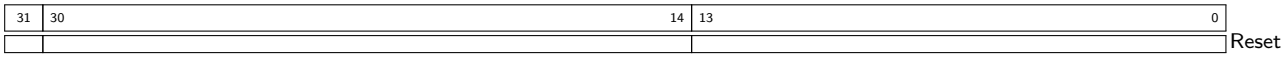
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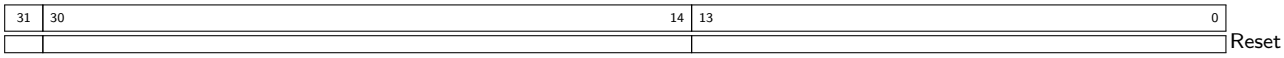
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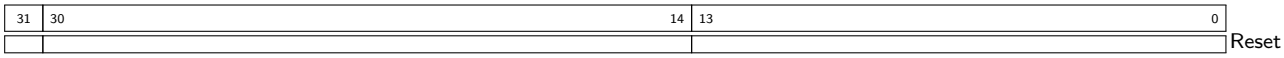
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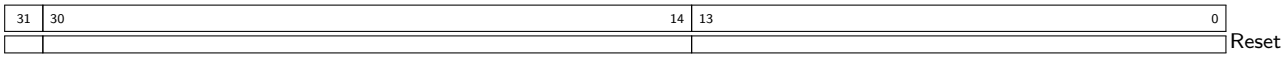
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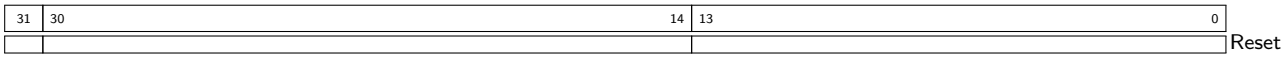
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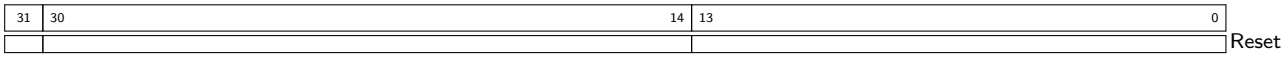
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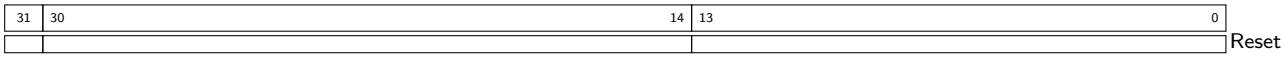
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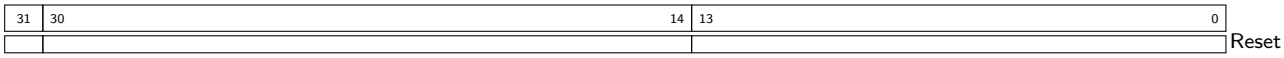
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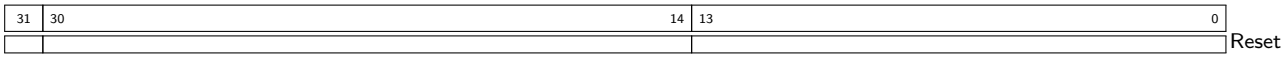
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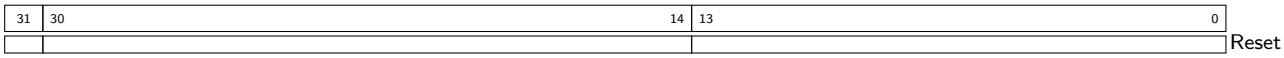
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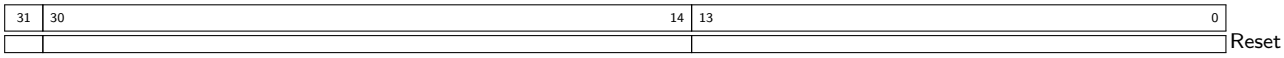
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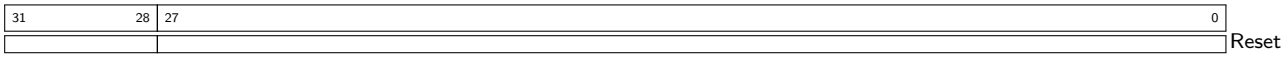
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28
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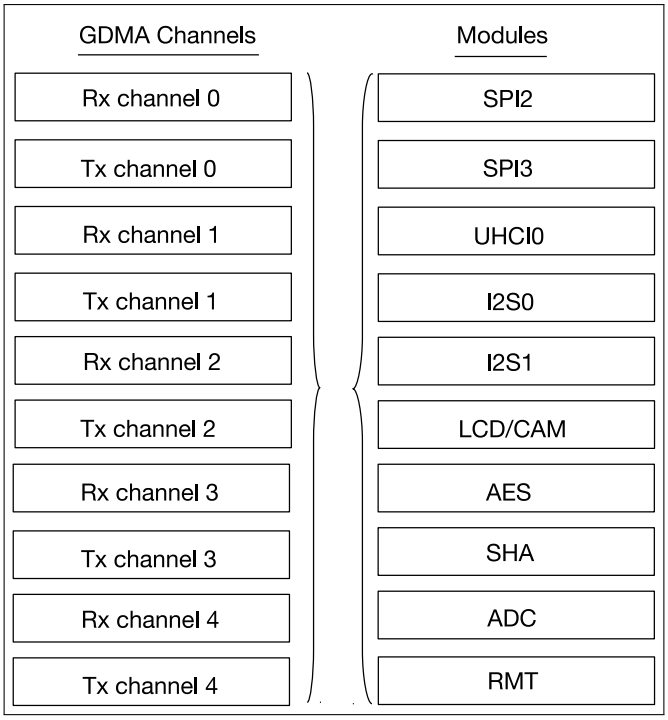
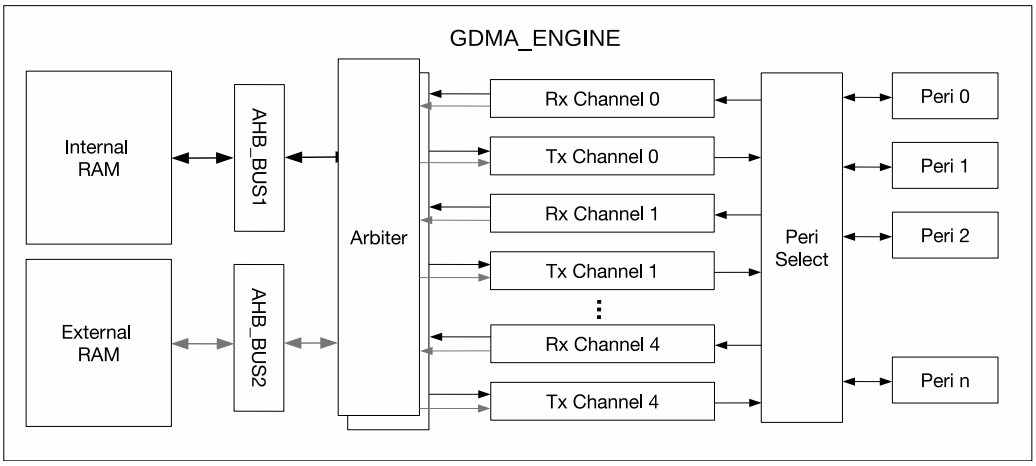
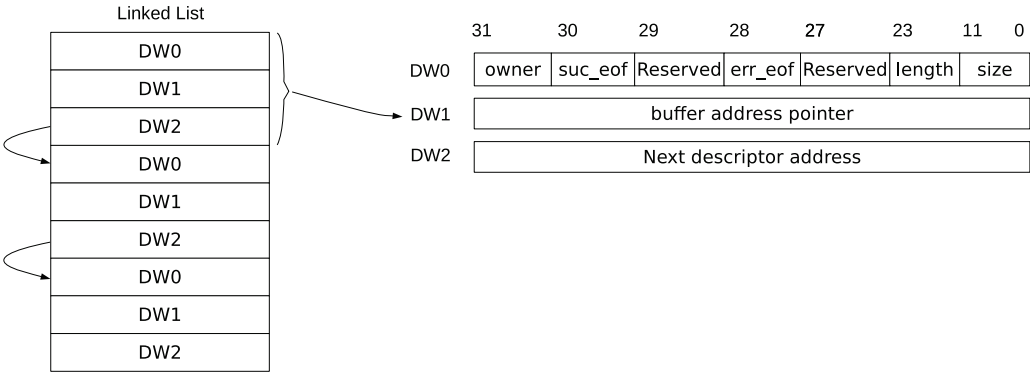

GDMA Channels
Modules
Rx channel 0
Tx channel 0
Rx channel 1
Tx channel 1
Rx channel 2
Tx channel 2
Rx channel 3
Tx channel 3
Rx channel 4
Tx channel 4
SPI2
SPI3
UHCI0
I2S0
I2S1
LCD/CAM
AES
SHA
ADC
RMT

-
-
-
-
-
-

-
-
-
-


GDMA_ENGINE
Internal RAM
External RAM
AHB_BUS1
AHB_BUS2
Arbiter
Rx Channel 0
Tx Channel 0
Rx Channel 1
Tx Channel 1
Rx Channel 4
Tx Channel 4
Peri Select
Peri 0
Peri 1
Peri 2
Peri n


Linked List
DW0
DW1
DW2
DW0
DW1
DW2
DW0
DW1
DW2
31
30
29
28
27
23
11
0
DW0
owner
suc_eof
Reserved
err_eof
Reserved
length
size
DW1
buffer address pointer
DW2
Next descriptor address

-
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-
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-
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-
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-
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-
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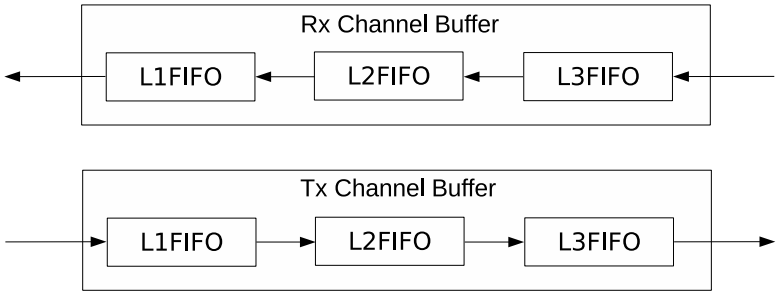
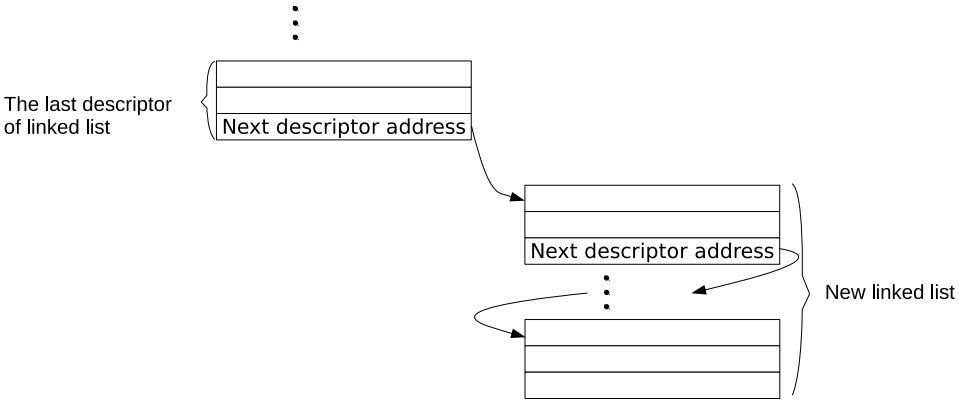
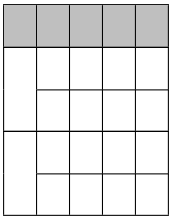
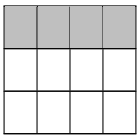

Rx Channel Buffer
L1FIFO
L2FIFO
L3FIFO
Tx Channel Buffer
L1FIFO
L2FIFO
L3FIFO


The last descriptor
of linked list
Next descriptor address
Next descriptor address
New linked list

-
-





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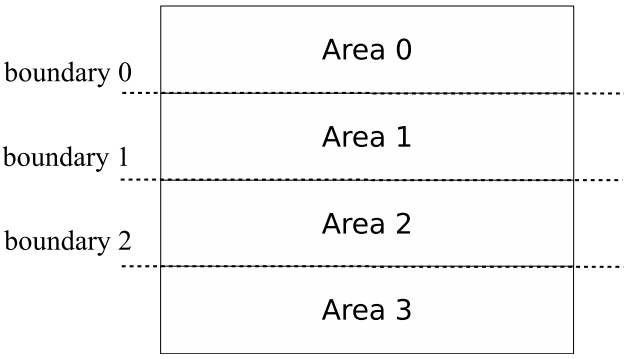
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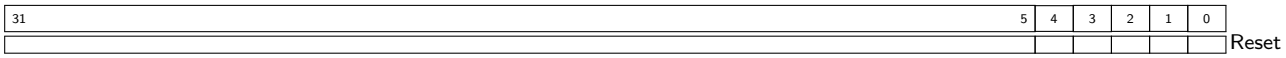
boundary 0
Area 1
boundary 1
Area 2
boundary 2
Area 3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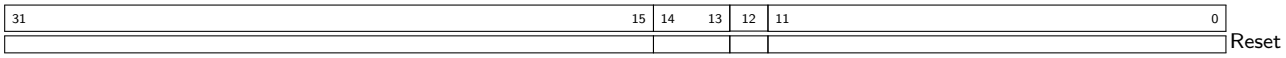
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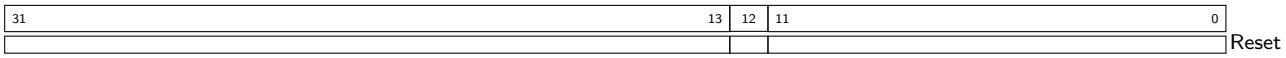
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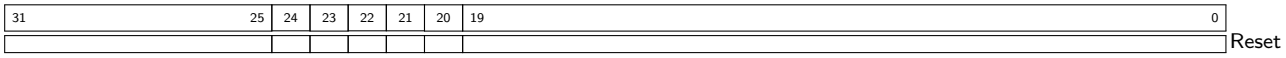
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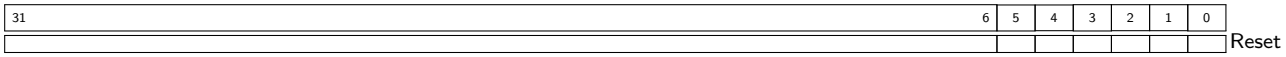
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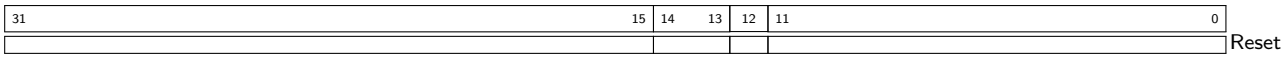
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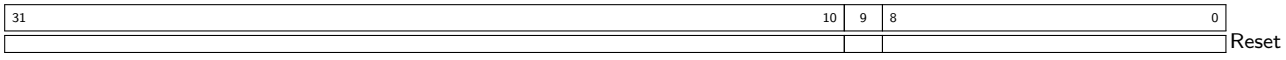
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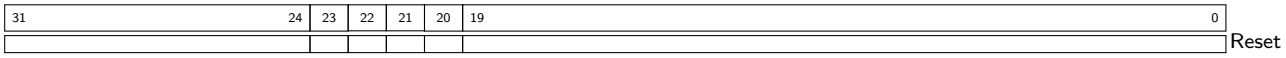
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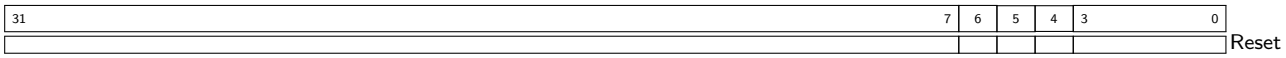
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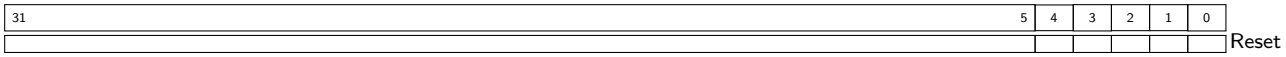
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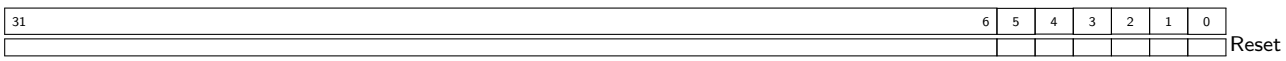
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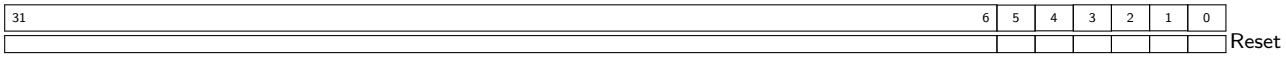
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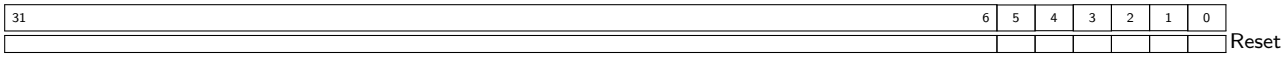
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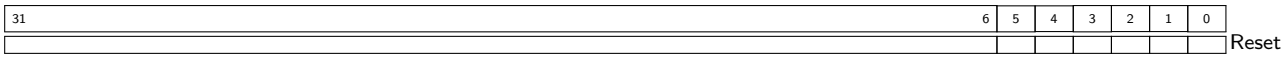
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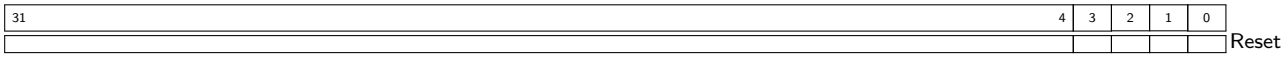
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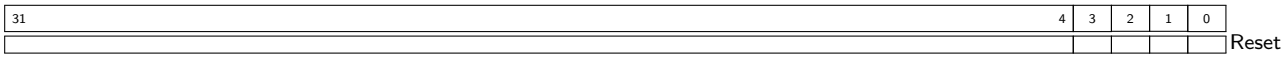
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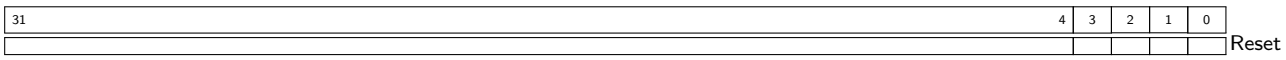
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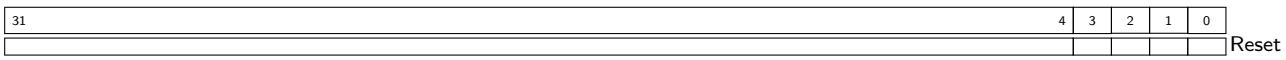
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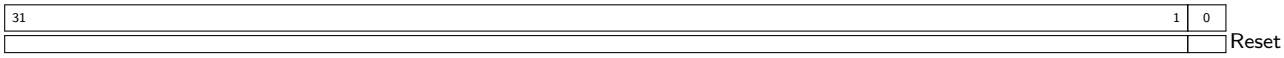
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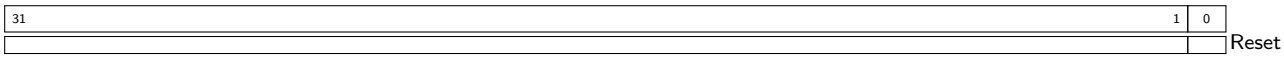
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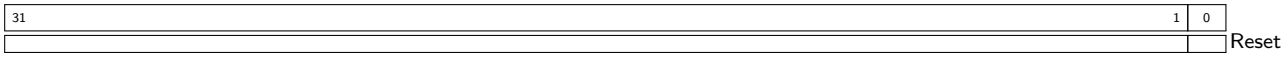
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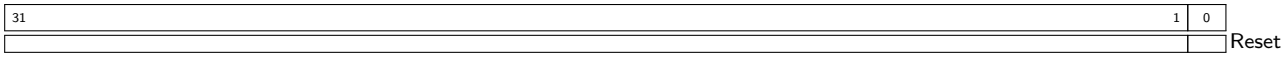
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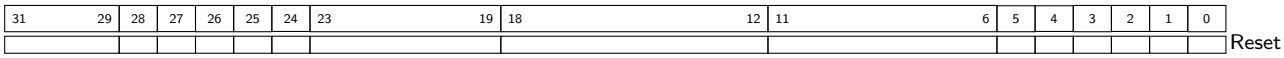
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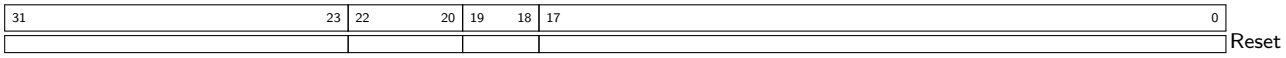
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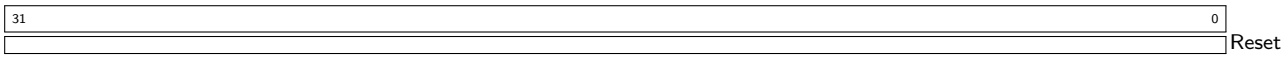
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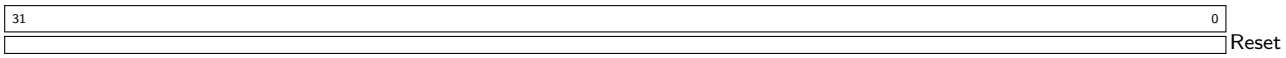
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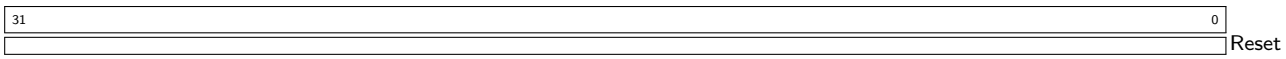
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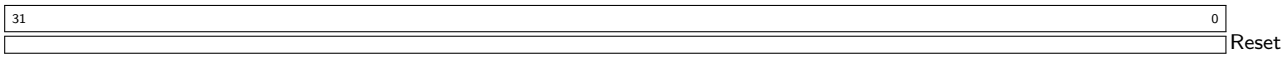
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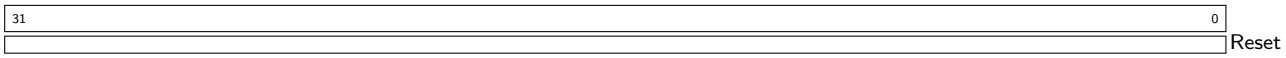
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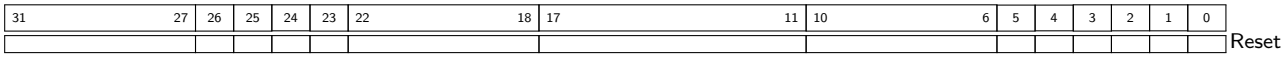
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0
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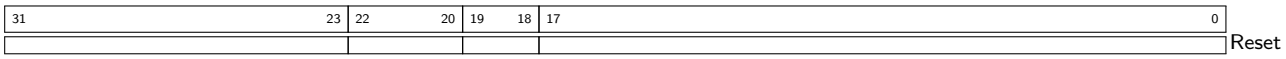
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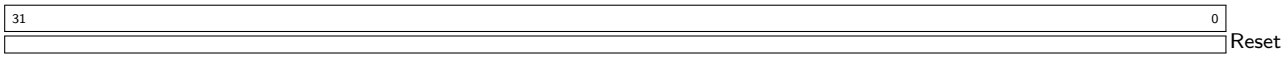
Reset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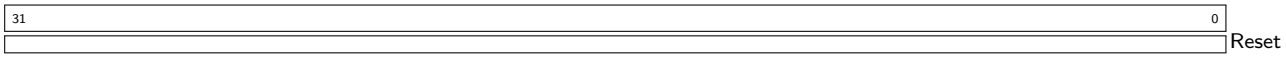
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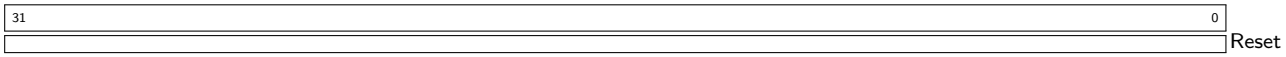
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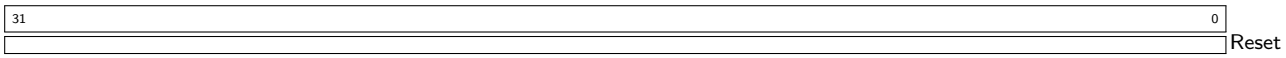
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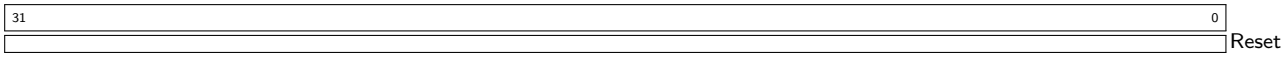
Reset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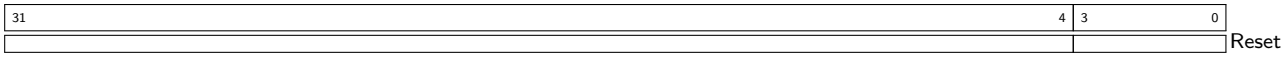
Reset


31
4
3
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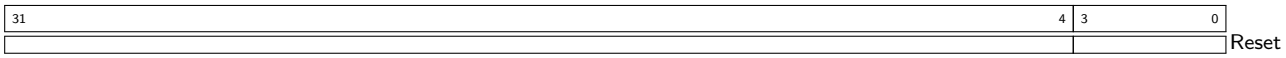
Reset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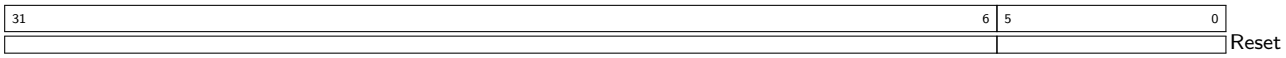
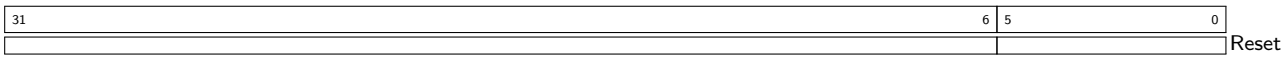
4
3
0
Reset


31
6
5
0
Reset


31
6
5
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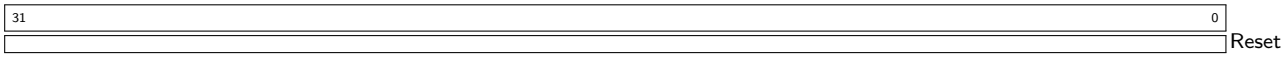
Reset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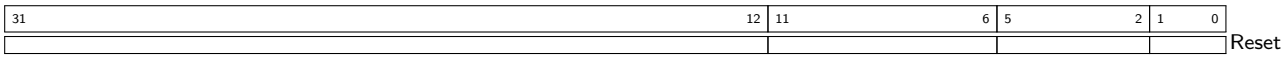
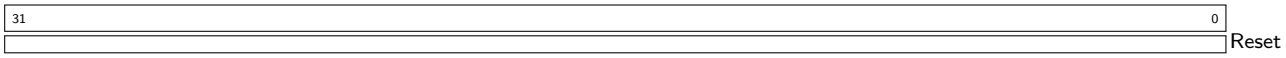
Reset


31
12
11
6
5
2
1
0
Reset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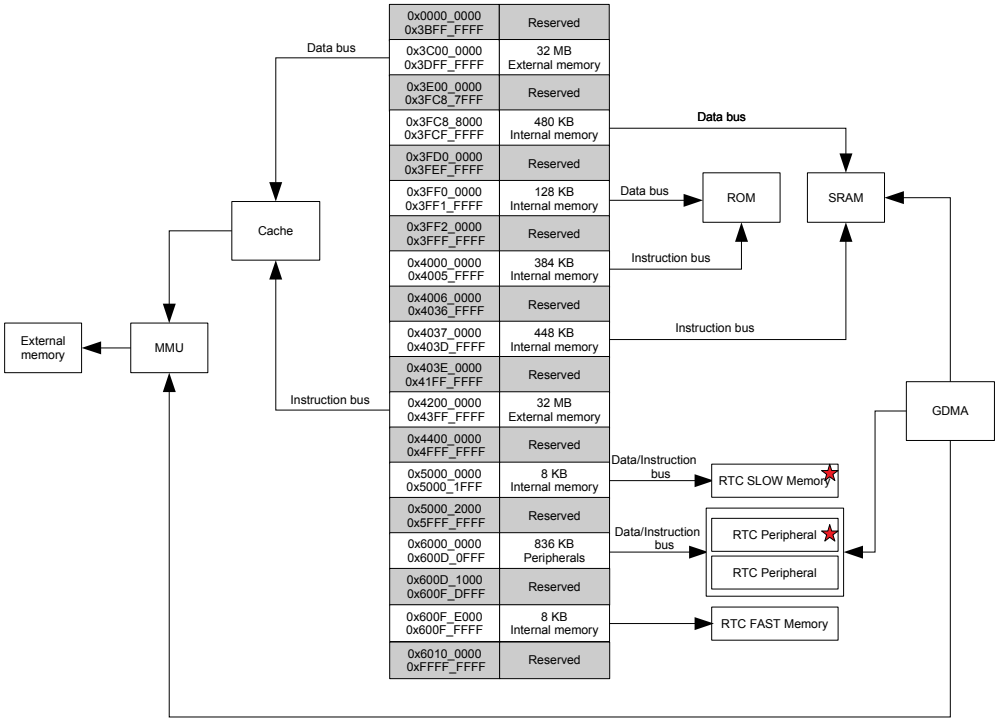
Reset


0x0000_0000 0x3BFF_FFFF
Reserved
0x3C00_0000 0x3DFF_FFFF
32 MB External memory
0x3E00_0000 0x3FC8_7FFF
Reserved
0x3FC8_8000 0x3FCF_FFFF
480 KB Internal memory
0x3FD0_0000 0x3FEF_FFFF
Reserved
0x3FF0_0000 0x3FF1_FFFF
128 KB Internal memory
0x3FF2_0000 0x3FFF_FFFF
Reserved
0x4000_0000 0x4005_FFFF
384 KB Internal memory
0x4006_0000 0x4036_FFFF
Reserved
0x4037_0000 0x403D_FFFF
448 KB Internal memory
0x403E_0000 0x41FF_FFFF
Reserved
0x4200_0000 0x43FF_FFFF
32 MB External memory
0x4400_0000 0x4FFF_FFFF
Reserved
0x5000_0000 0x5000_1FFF
8 KB Internal memory
0x5000_2000 0x5FFF_FFFF
Reserved
0x6000_0000 0x600D_0FFF
836 KB Peripherals
0x600D_1000 0x600F_DFFF
Reserved
0x600F_E000 0x600F_FFFF
8 KB Internal memory
0x6010_0000 0xFFFF_FFFF
Reserved
Data bus
Data bus
Data bus
ROM
SRAM
Instruction bus
Instruction bus
Cache
External memory
MMU
Instruction bus
GDMA
Data/Instruction bus
RTC SLOW Memory
Data/Instruction bus
RTC Peripheral
RTC Peripheral
RTC FAST Memory

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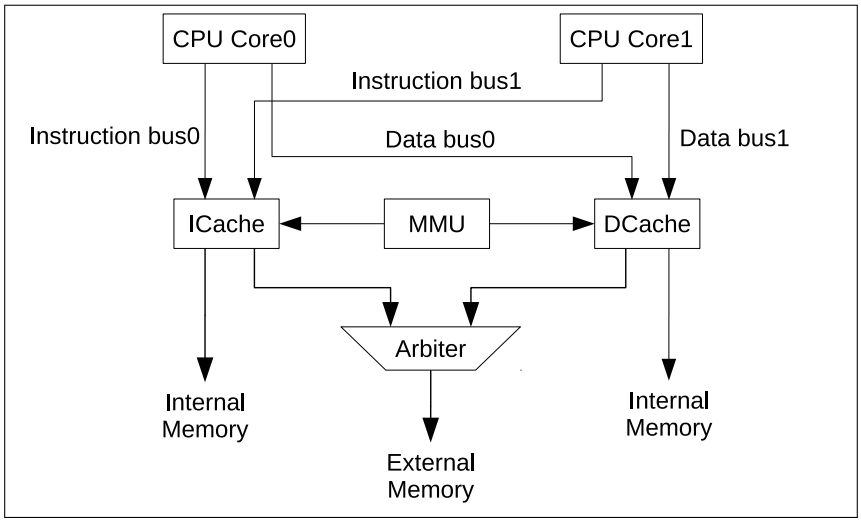
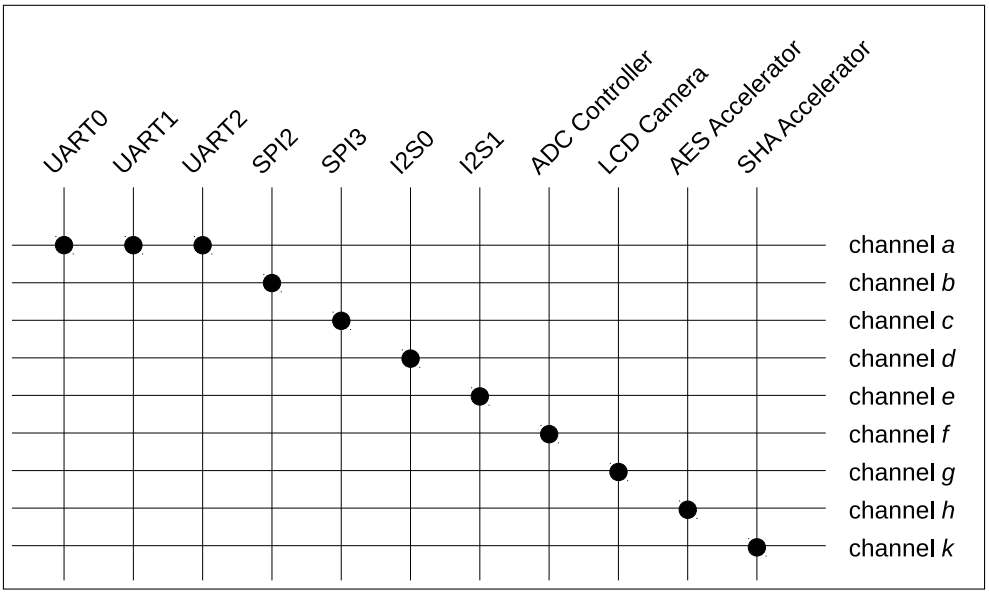
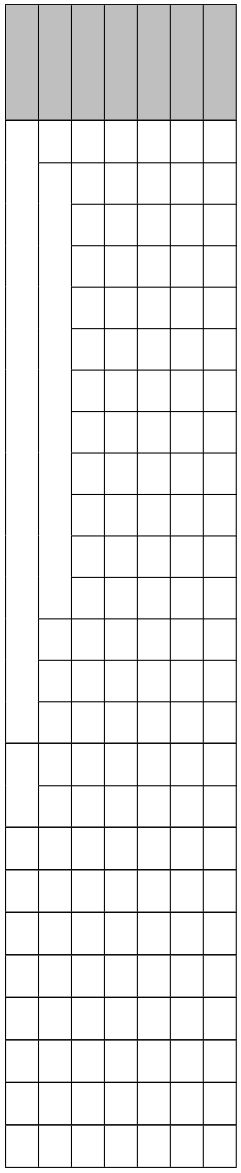

CPU Core0
CPU Core1
Instruction bus1
Instruction bus0
Data bus0
Data bus1
ICache
MMU
DCache
Arbiter
Internal
Memory
Internal
Memory
External
Memory

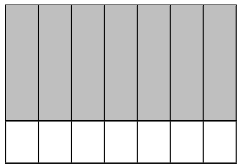
-
-
-

-

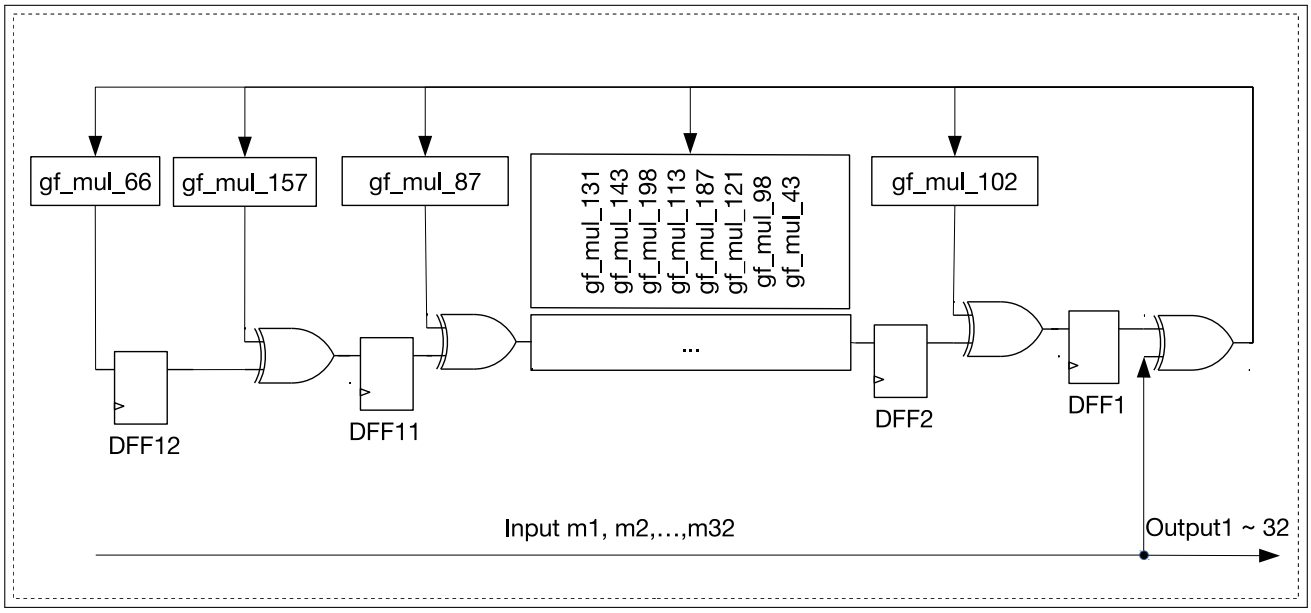

UART0
UART1
UART2
SPI2
SPI3
I2S0
I2S1
ADC Controller
LCD Camera
AES Accelerator
SHA Accelerator
channel a
channel b
channel c
channel d
channel e
channel f
channel g
channel h
channel k

-
-
-
-
-





$p(x) = x^8 + x^4 + x^3 + x^2 + 1$



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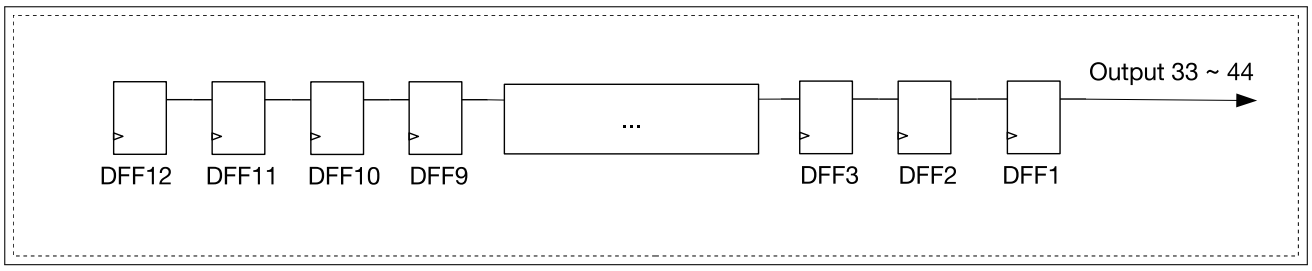
Output 33 ~ 44
...
DFF12
DFF11
DFF10
DFF9
DFF3
DFF2
DFF1

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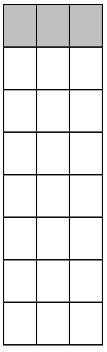

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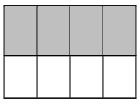

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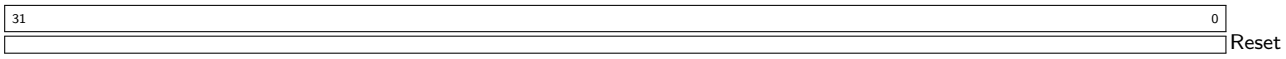
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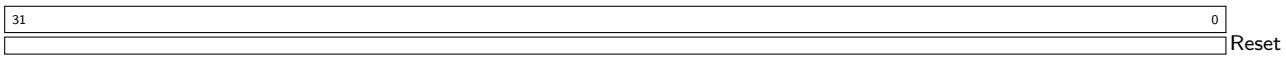
Reset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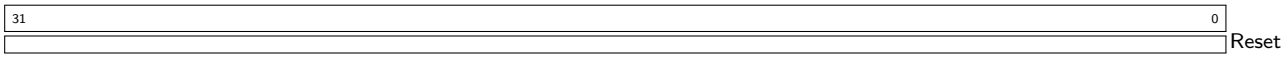
Reset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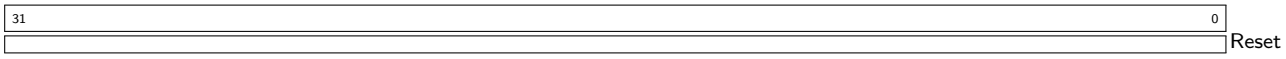
Reset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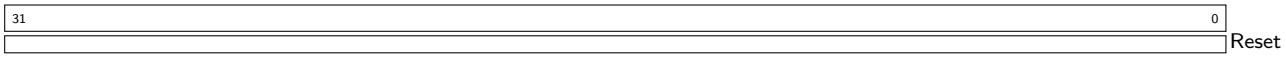
Reset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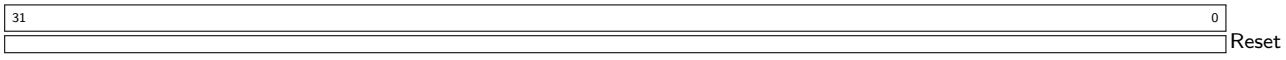
Reset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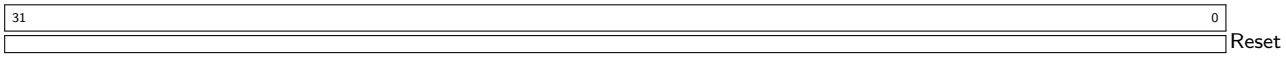
Reset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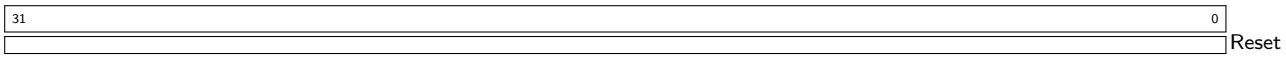
Reset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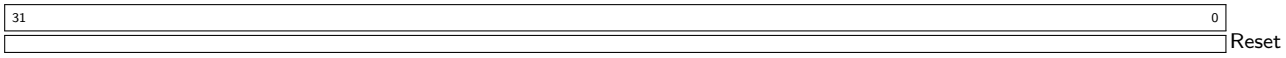
Reset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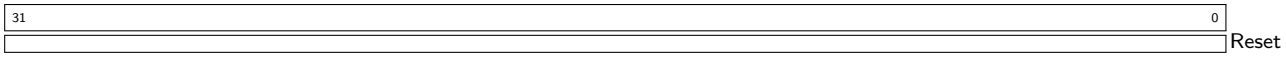
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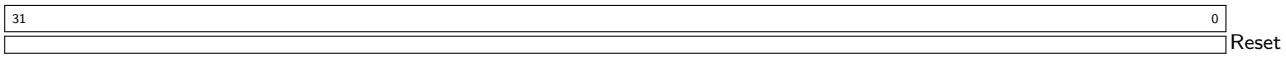
Reset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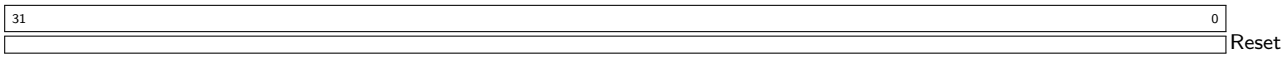
Reset


31
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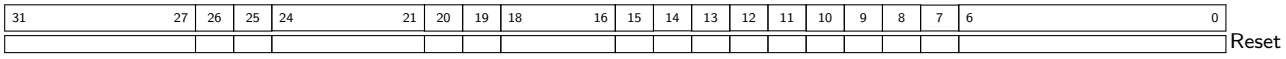
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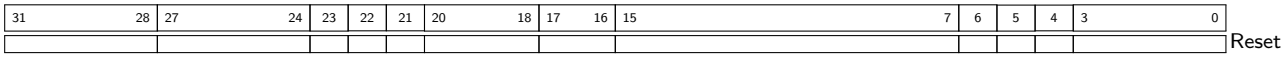
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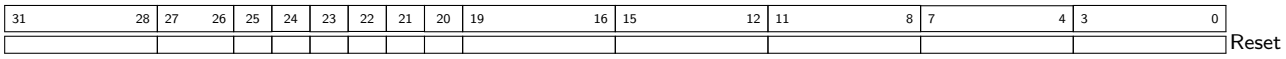
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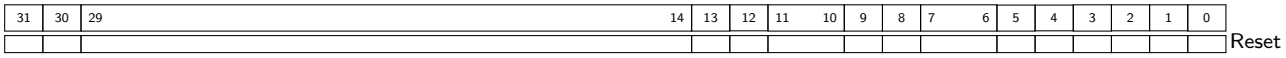
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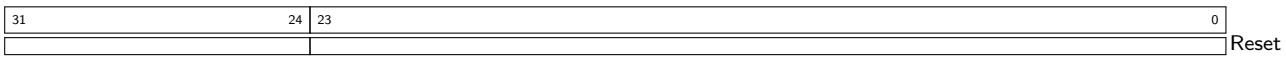
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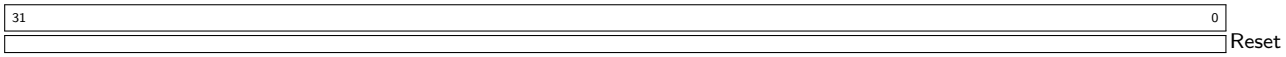
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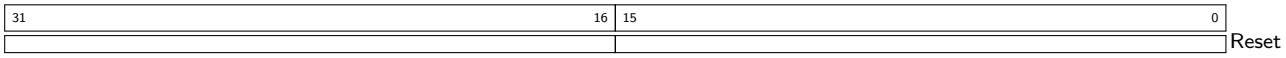
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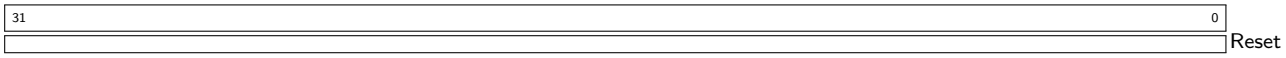
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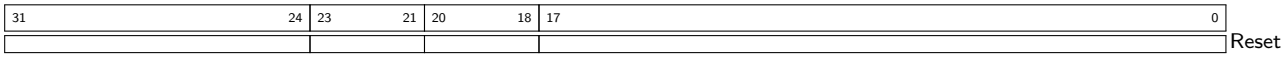
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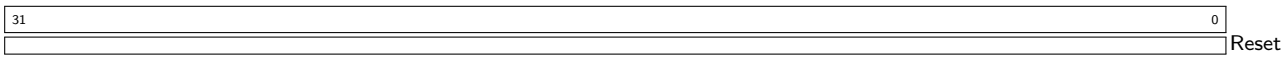
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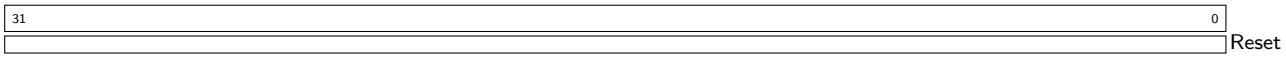
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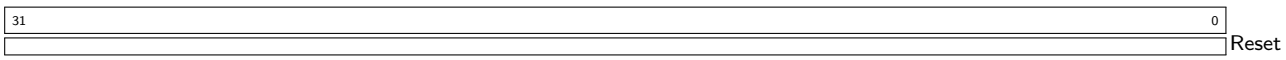
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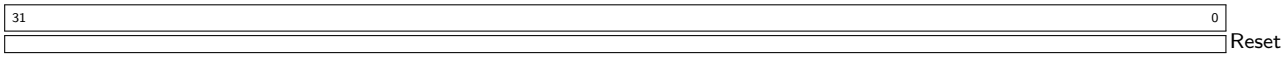
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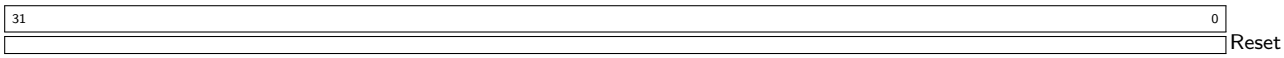
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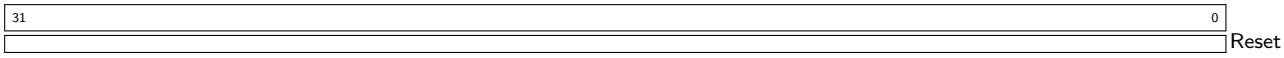
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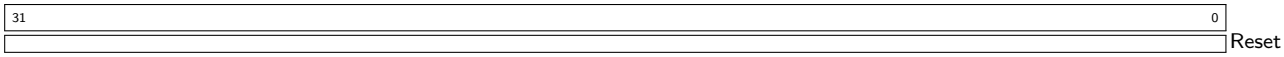
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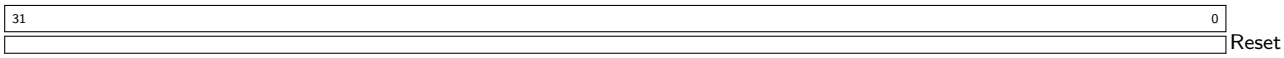
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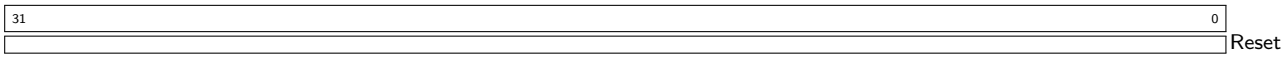
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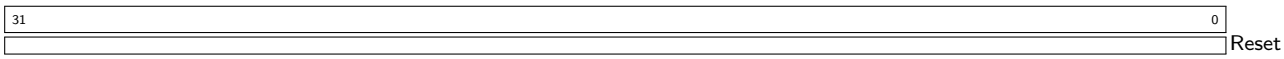
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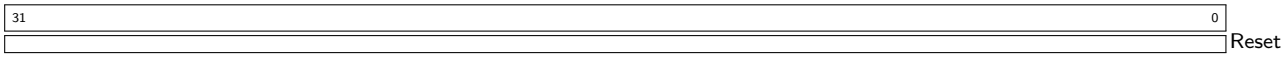
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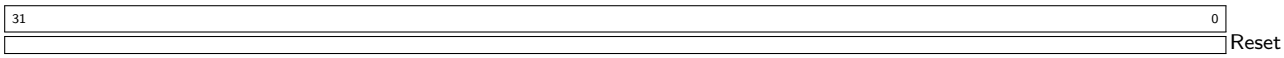
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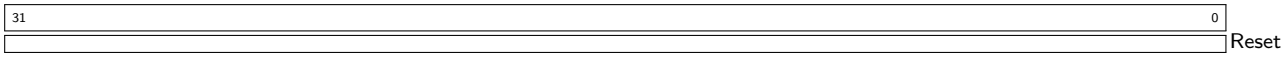
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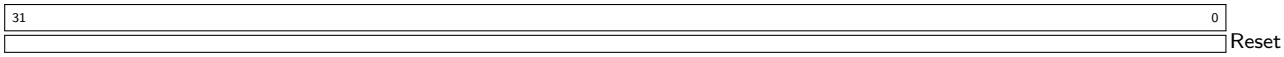
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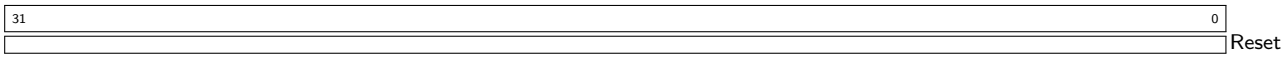
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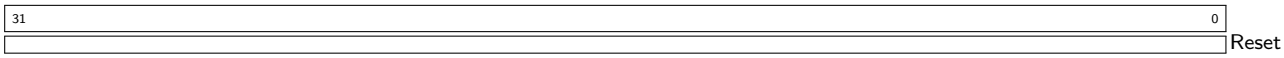
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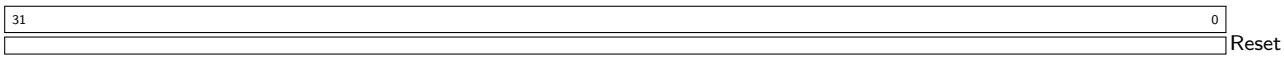
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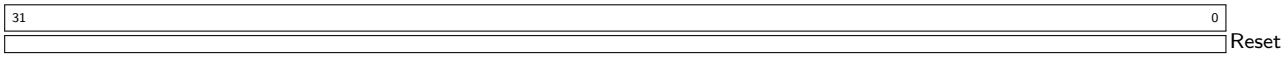
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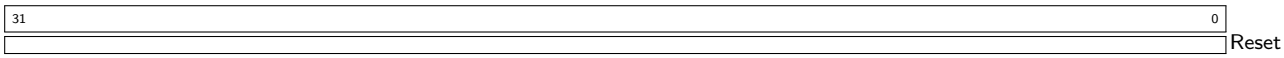
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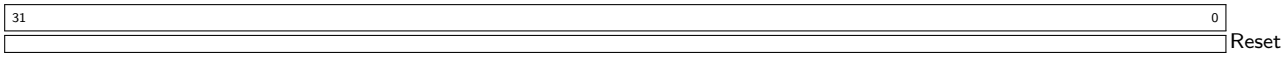
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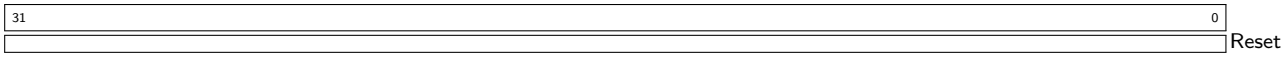
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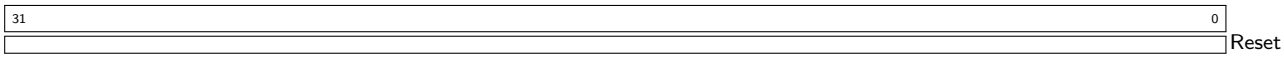
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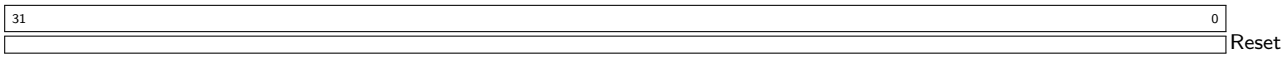
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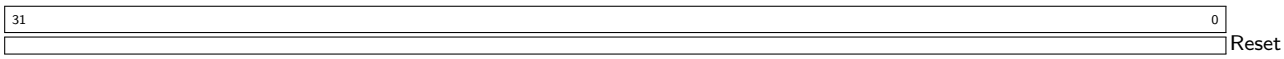
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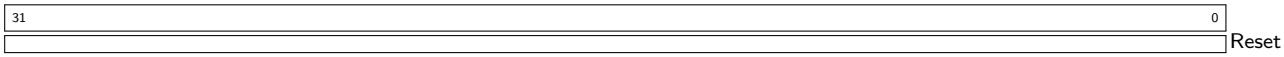
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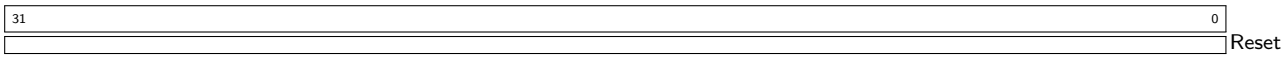
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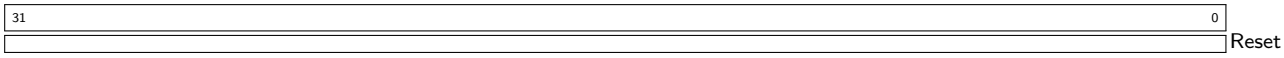
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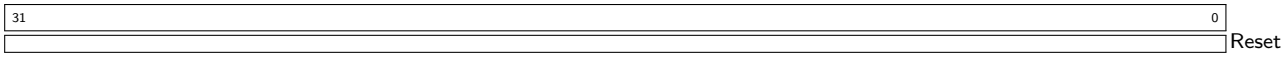
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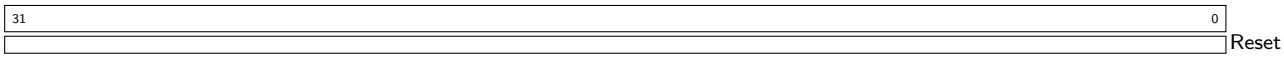
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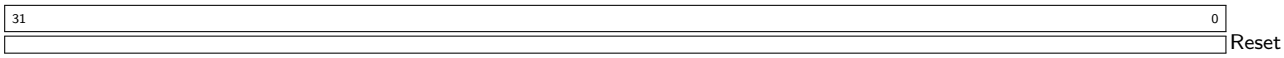
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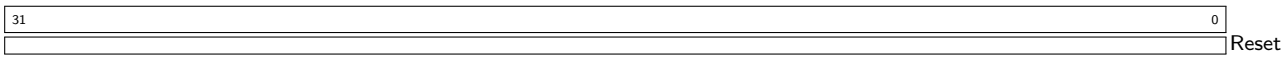
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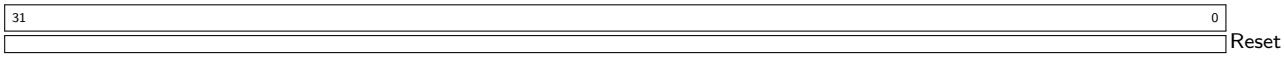
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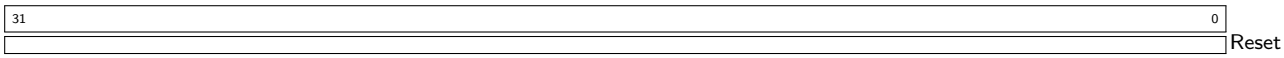
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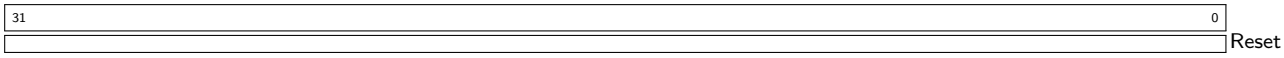
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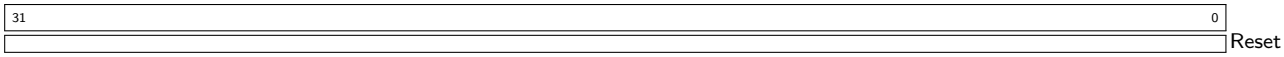
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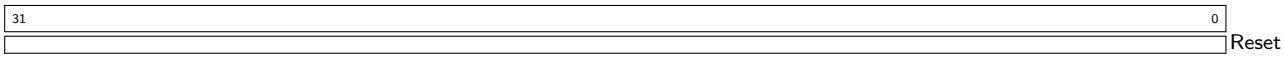
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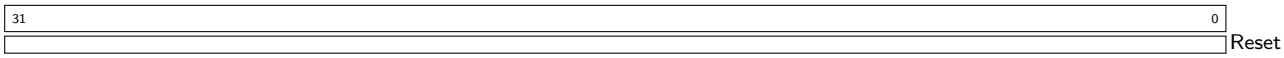
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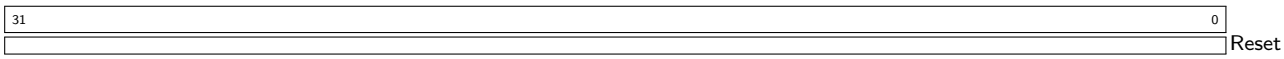
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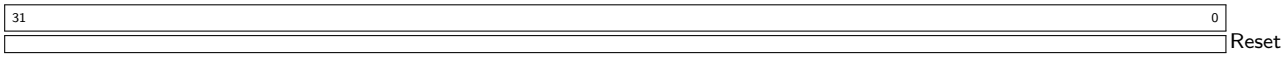
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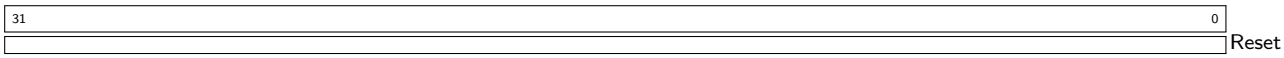
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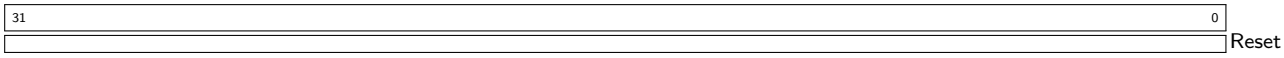
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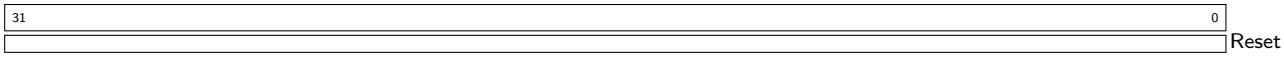
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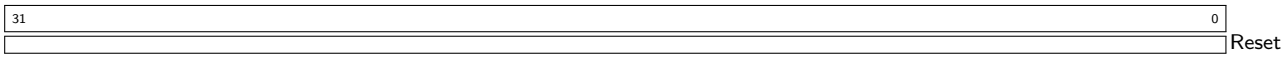
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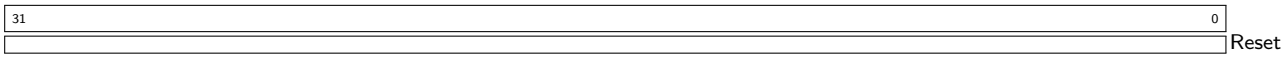
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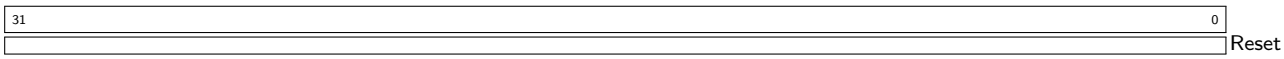
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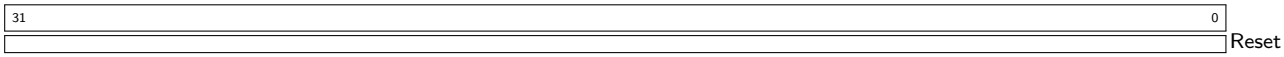
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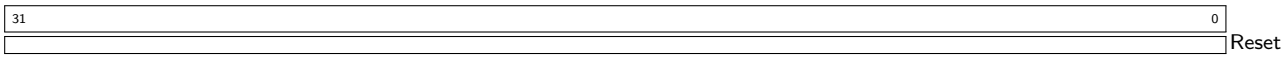
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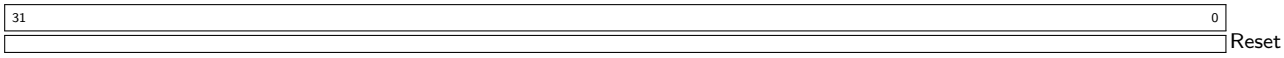
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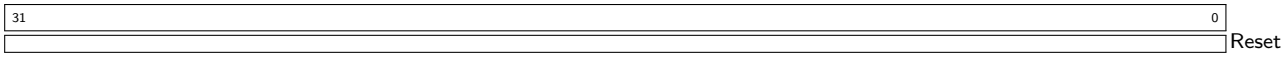
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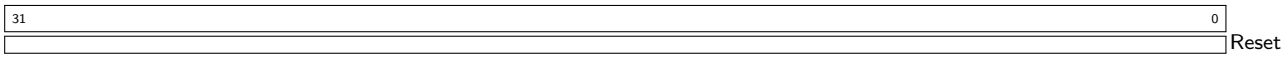
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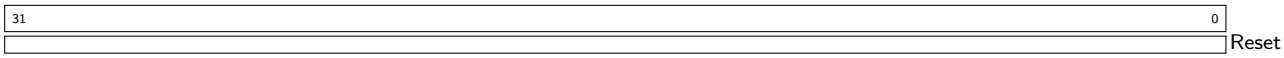
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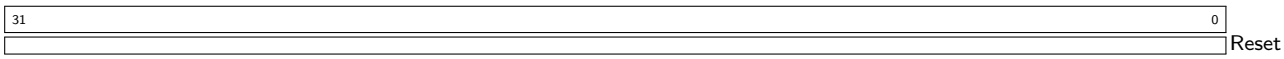
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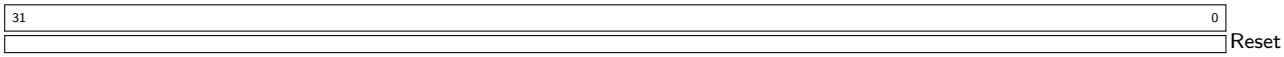
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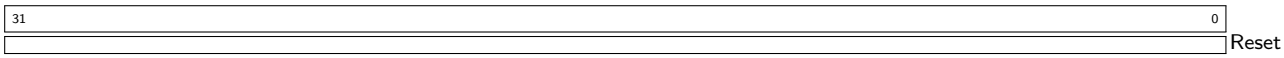
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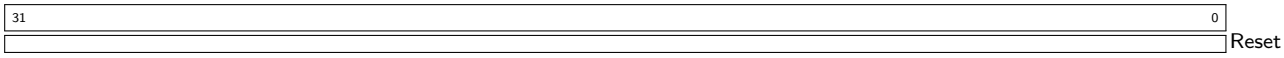
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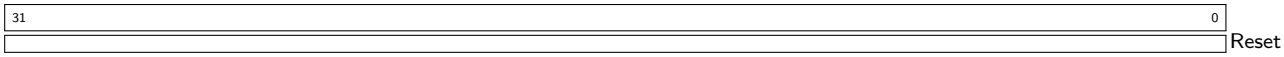
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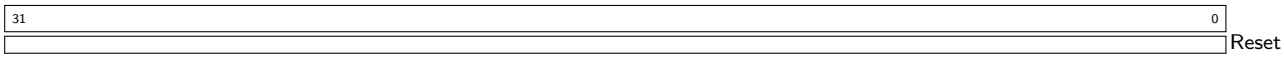
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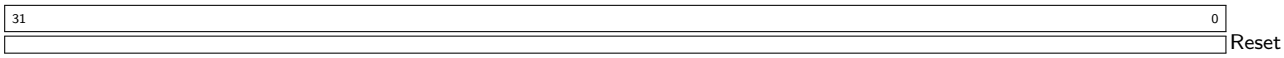
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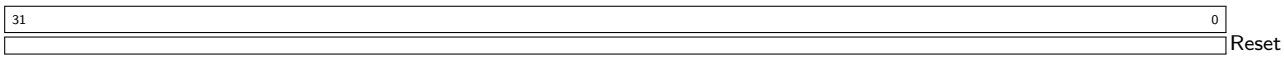
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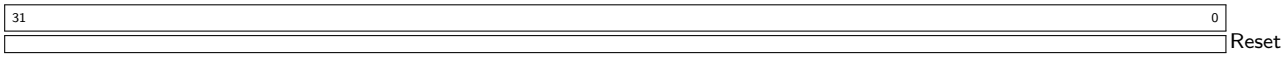
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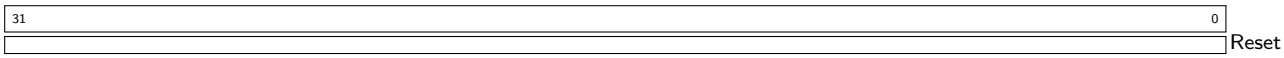
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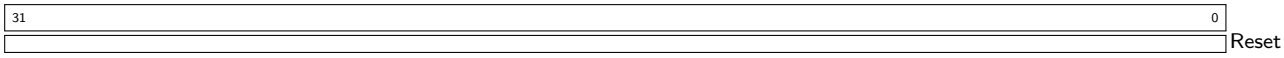
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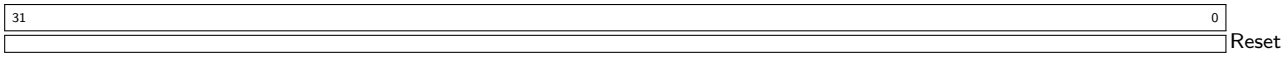
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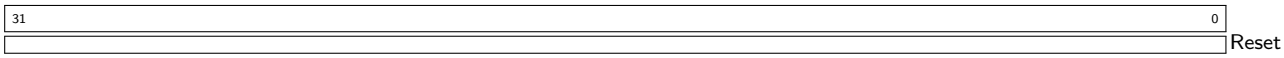
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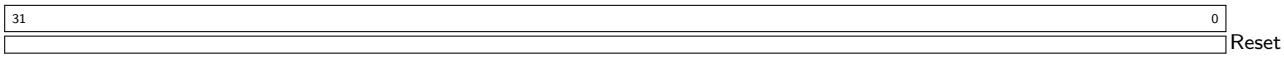
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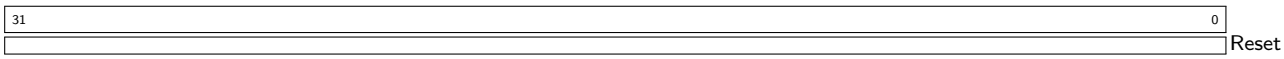
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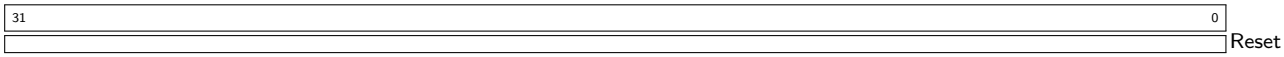
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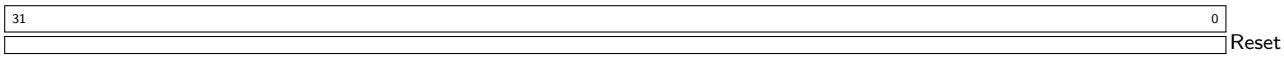
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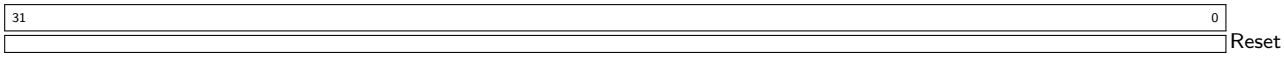
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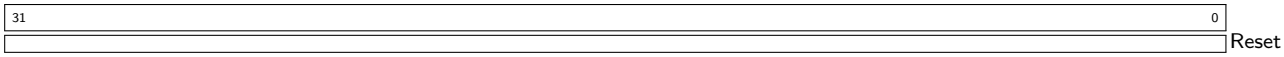
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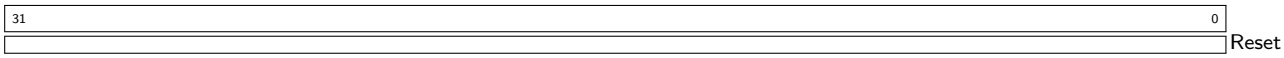
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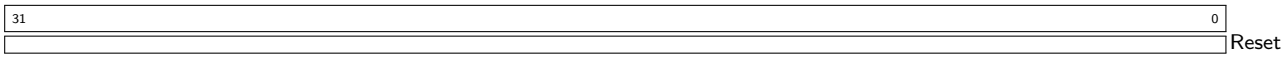
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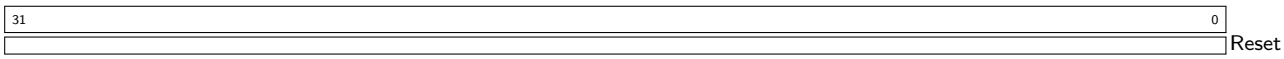
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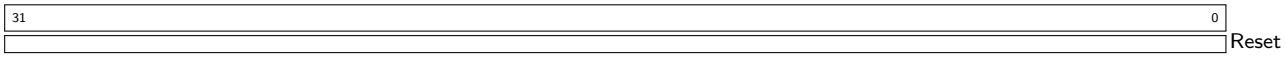
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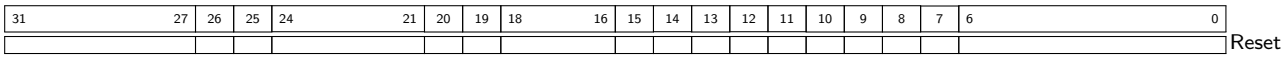
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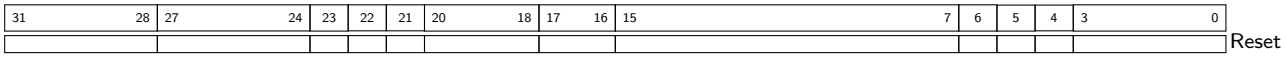
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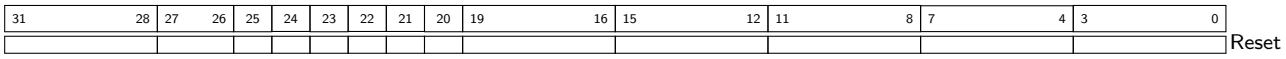
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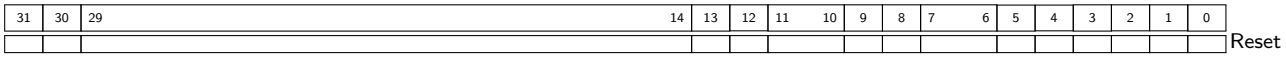
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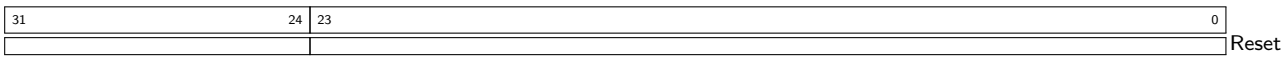
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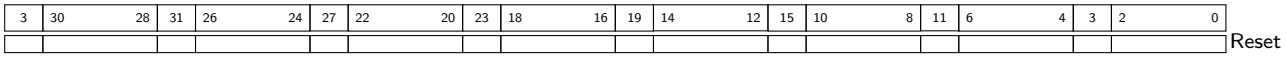
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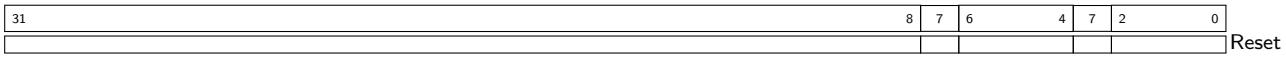
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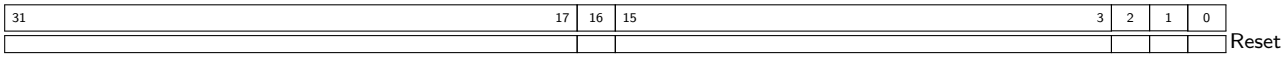
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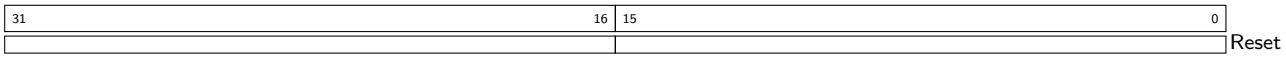
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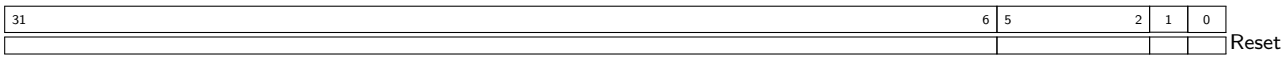
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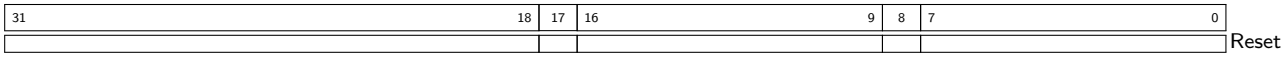
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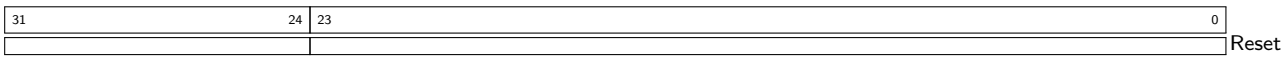
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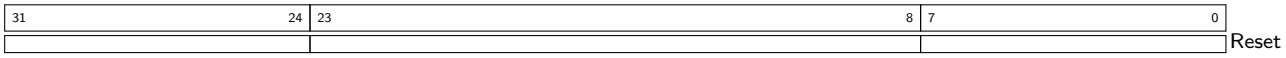
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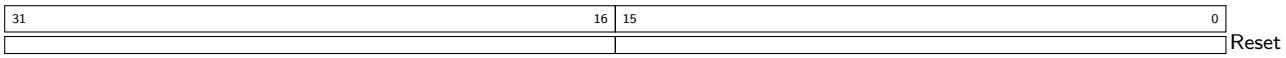
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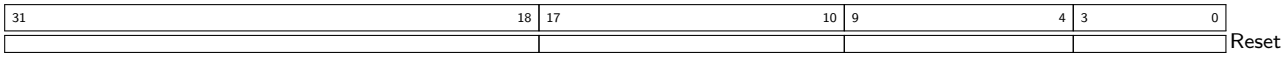
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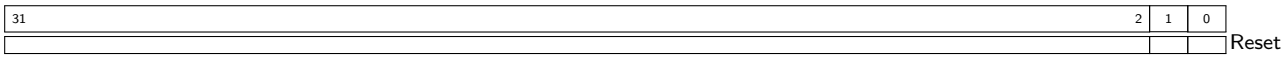
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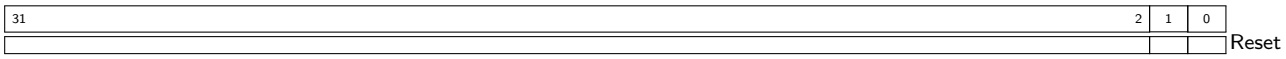
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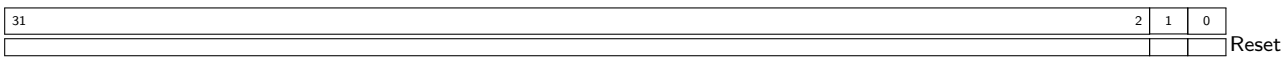
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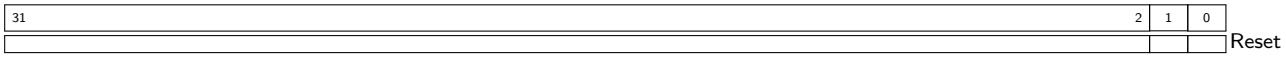
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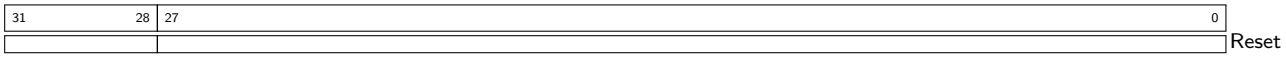
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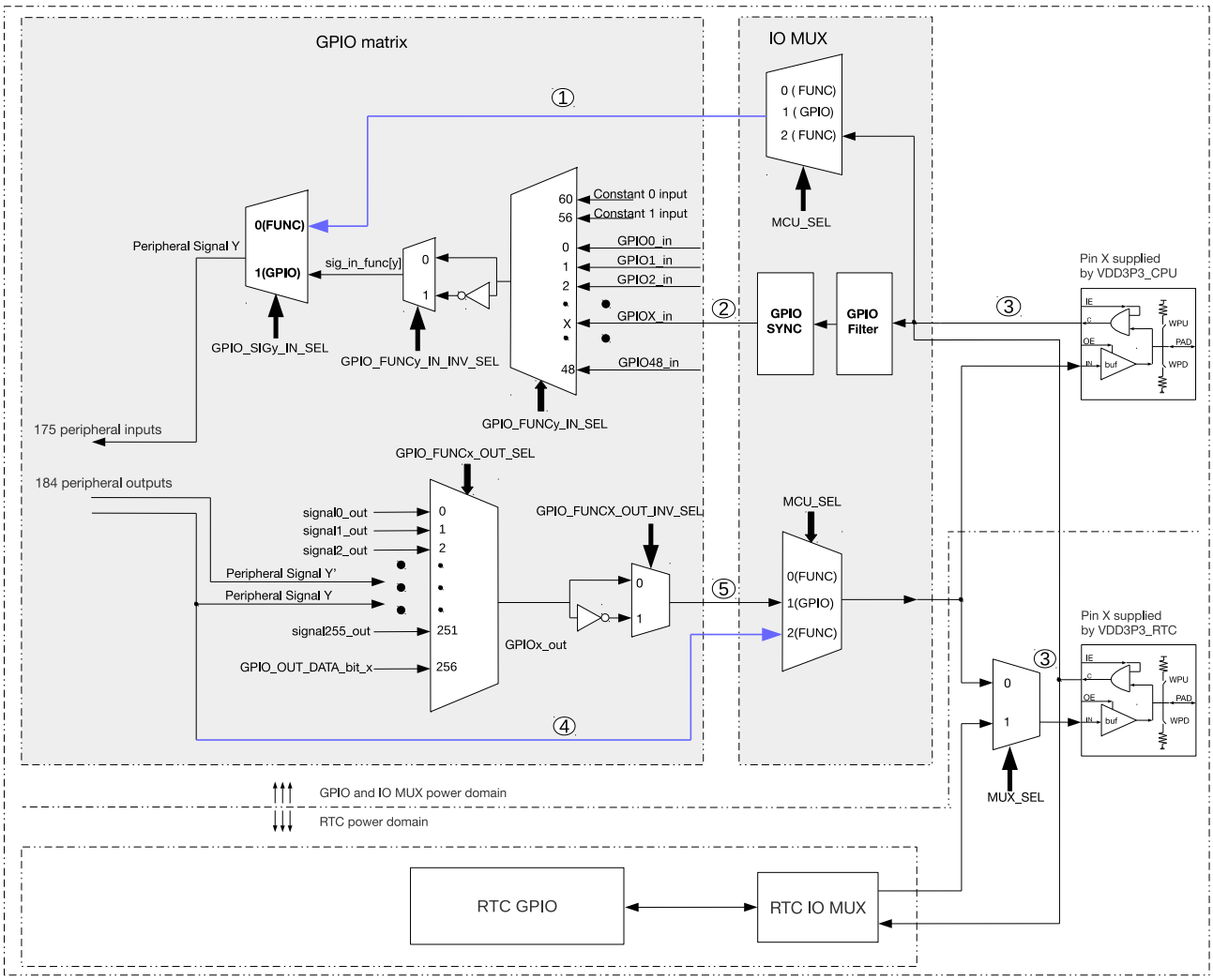
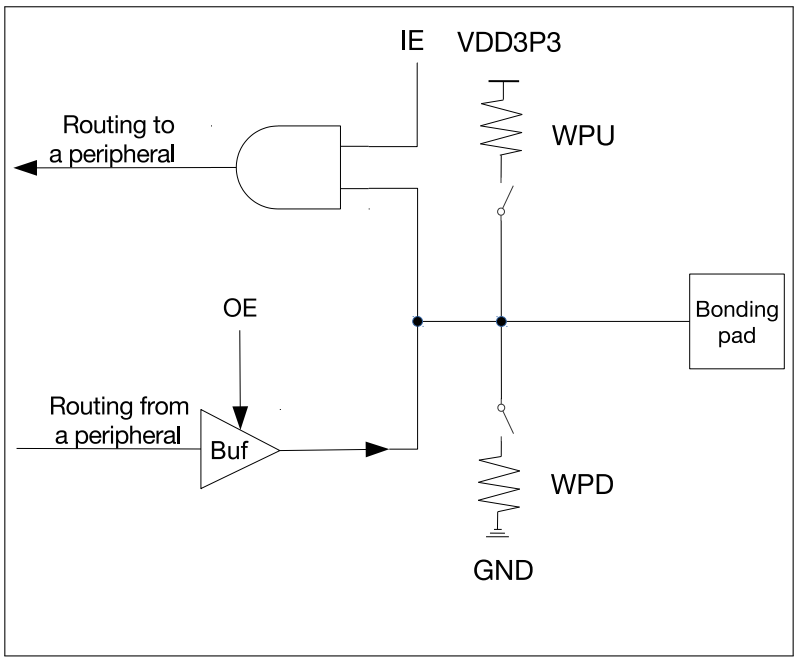

GPIO matrix
IO MUX
0 (FUNC)
1 (GPIO)
2 (FUNC)
MCU_SEL
Peripheral Signal Y
0(FUNC)
1(GPIO)
sig_in_func[y]
GPIO_SIGy_IN_SEL
GPIO_FUNCy_IN_INV_SEL
Constant 0 input
Constant 1 input
GPIO0_in
GPIO1_in
GPIO2_in
GPIOX_in
GPIO48_in
GPIO_FUNCy_IN_SEL
GPIO SYNC
GPIO Filter
Pin X supplied by VDD3P3_CPU
175 peripheral inputs
184 peripheral outputs
GPIO_FUNCx_OUT_SEL
signal0_out
signal1_out
signal2_out
Peripheral Signal Y'
Peripheral Signal Y
signal255_out
GPIO_OUT_DATA_bit_x
GPIO_FUNCX_OUT_INV_SEL
GPIOx_out
MCU_SEL
0(FUNC)
1(GPIO)
2(FUNC)
Pin X supplied by VDD3P3_RTC
MUX_SEL
GPIO and IO MUX power domain
RTC power domain
RTC GPIO
RTC IO MUX


IE
VDD3P3
Routing to
a peripheral
WPU
OE
Bonding
pad
Routing from
a peripheral
Buf
WPD
GND

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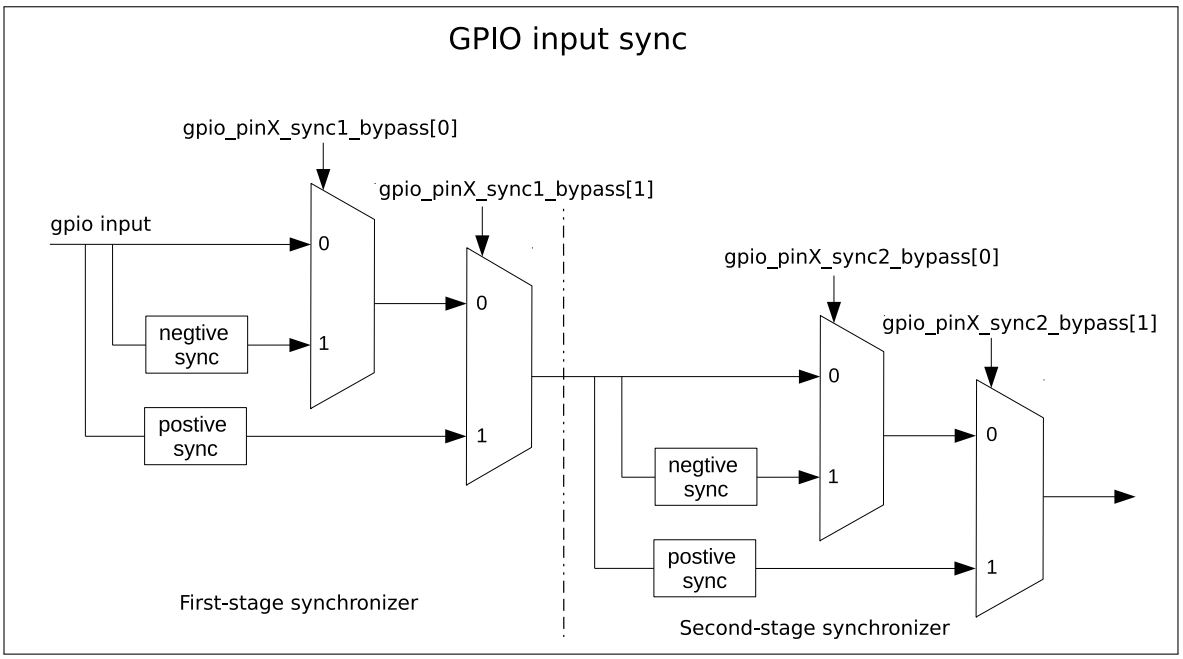
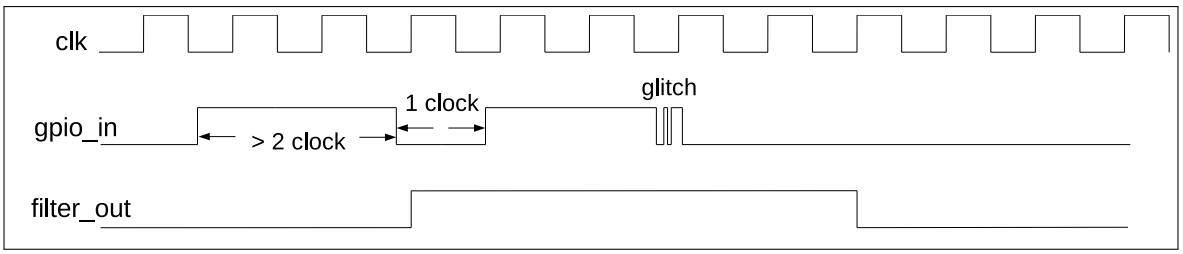

GPIO input sync
gpio_pinX_sync1_bypass[0]
gpio_pinX_sync1_bypass[1]
gpio input
0
1
negtive sync
postive sync
0
1
gpio_pinX_sync2_bypass[0]
gpio_pinX_sync2_bypass[1]
0
1
negtive sync
postive sync
0
1
First-stage synchronizer
Second-stage synchronizer

1

-
-


clk
gpio_in
1 clock
glitch
> 2 clock
filter_out

-
-
- 2

-

[3]

-
-

[1,2]

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-
-

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-

$$H(z) = {}^{-1} + {}^{-12}$$

-
-

1

- 0
- 50
- 100

$$DutyCycle = \frac{GPIOSDIN + 128}{256}$$

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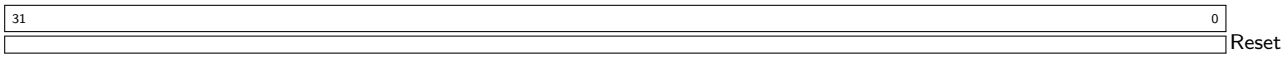
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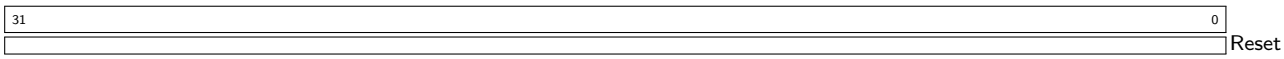
Reset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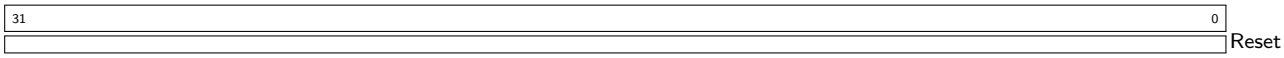
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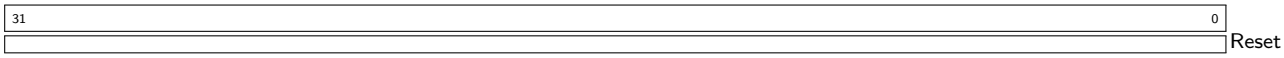
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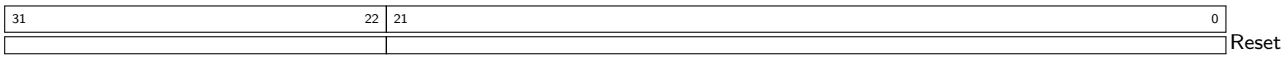
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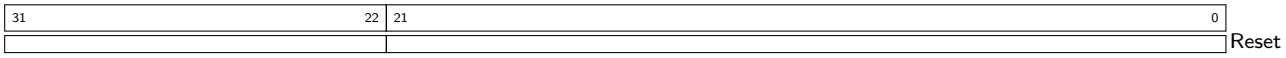
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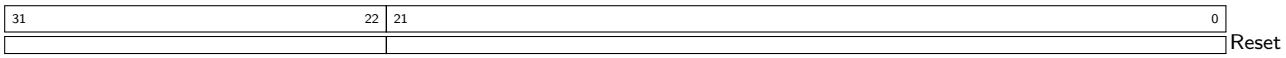
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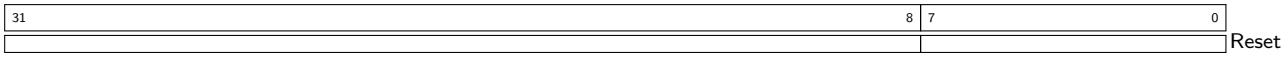
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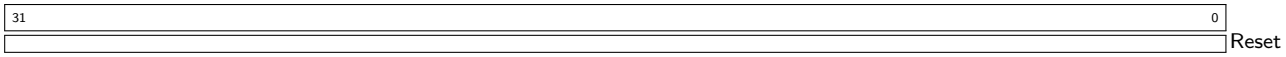
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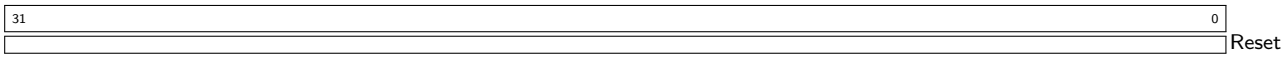
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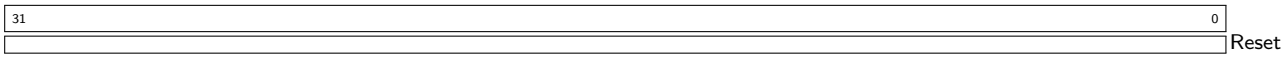
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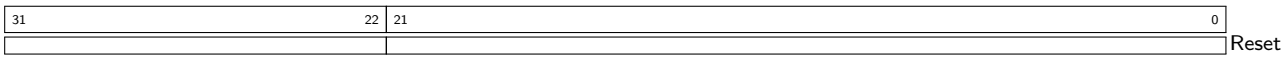
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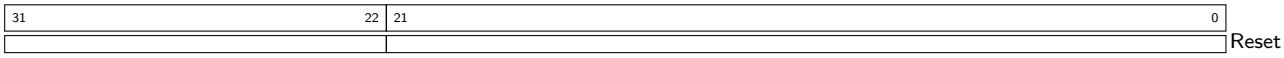
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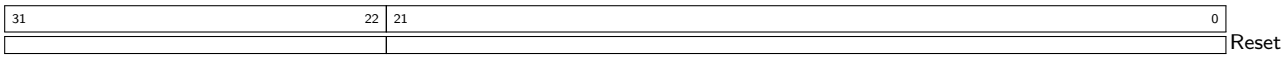
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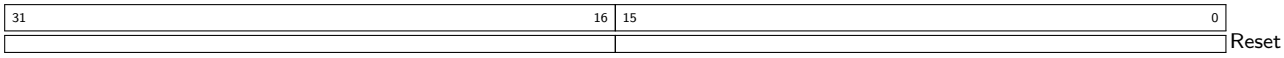
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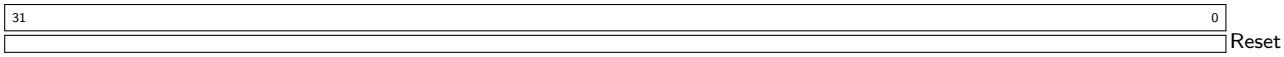
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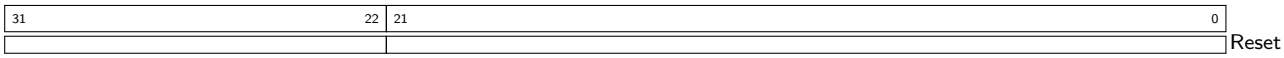
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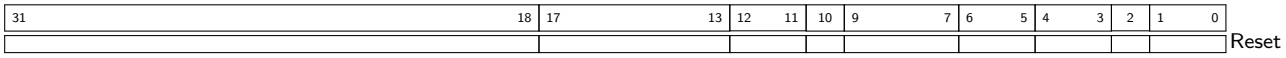
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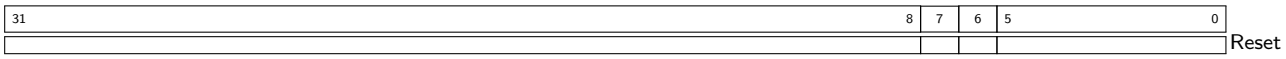
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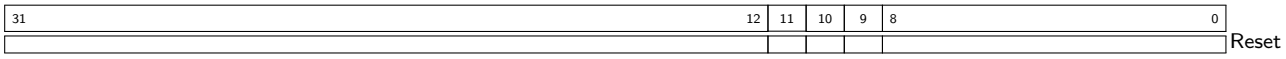
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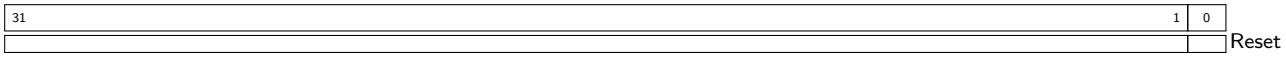
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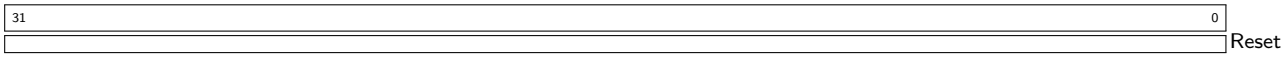
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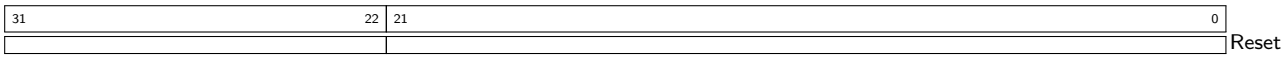
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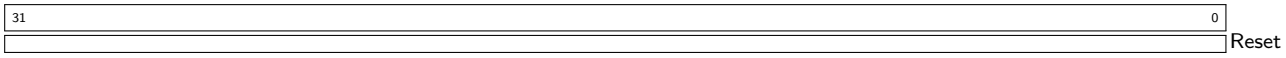
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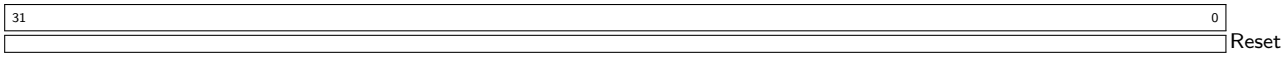
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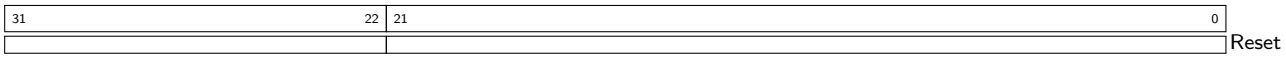
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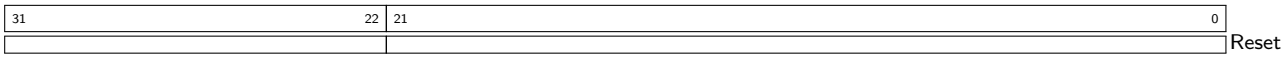
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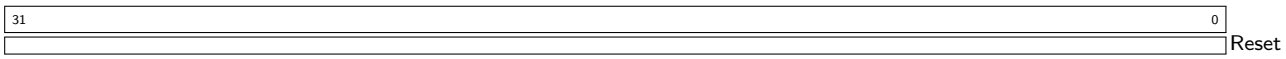
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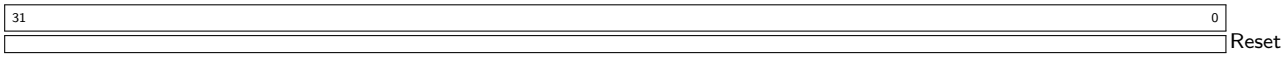
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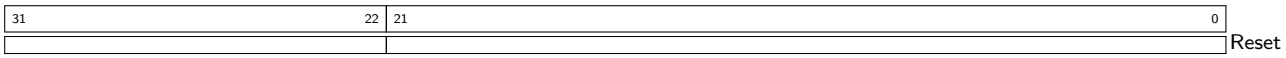
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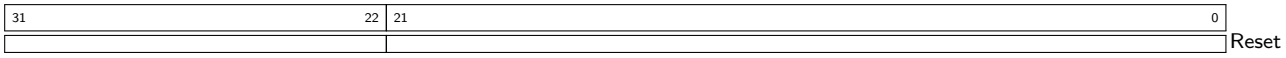
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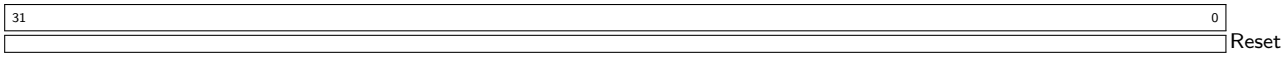
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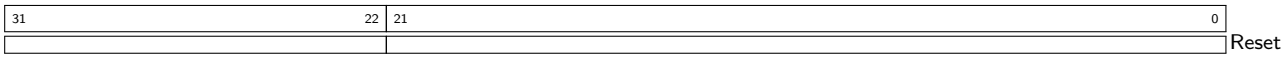
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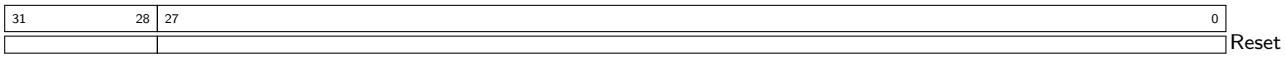
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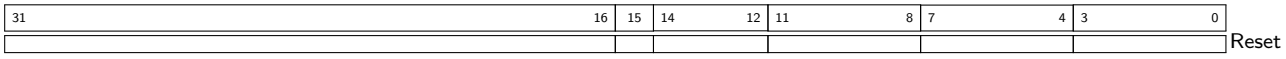
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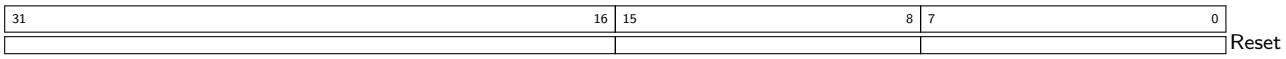
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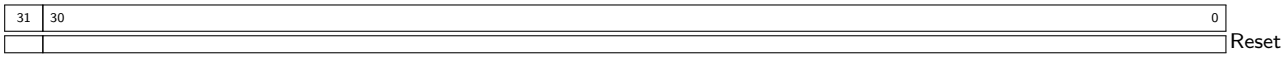
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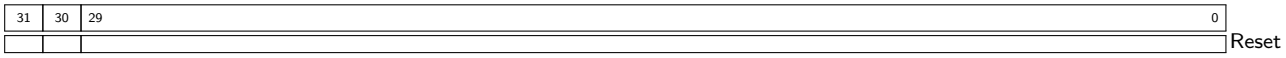
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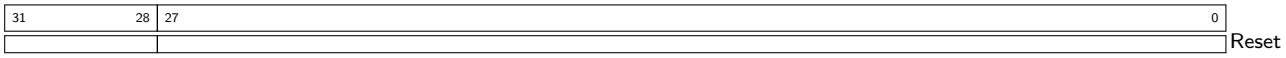
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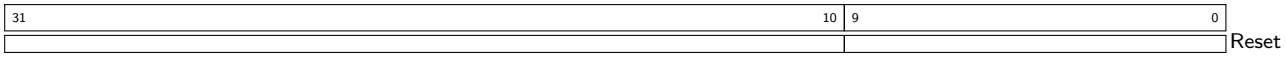
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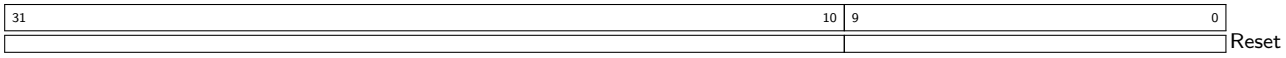
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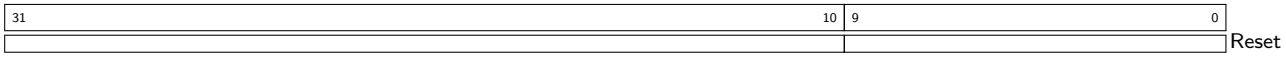
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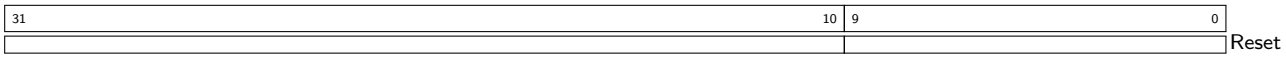
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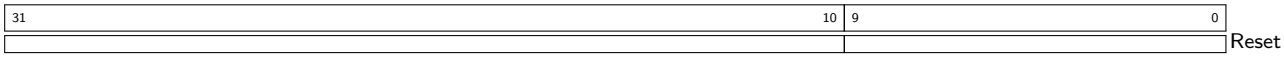
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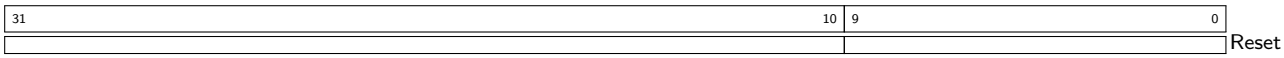
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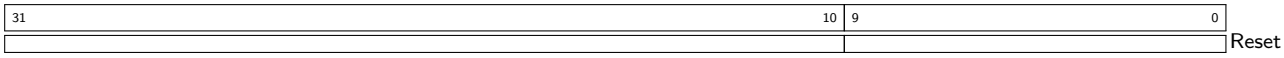
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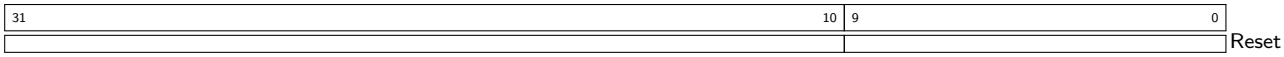
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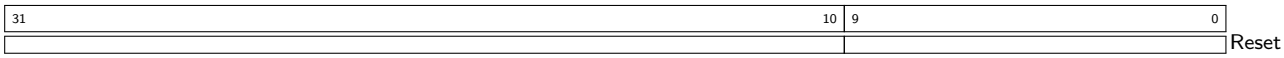
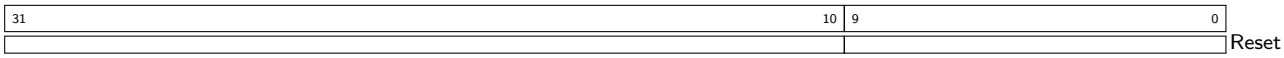
10
9
0
Reset


31
10
9
0
Reset


31
10
9
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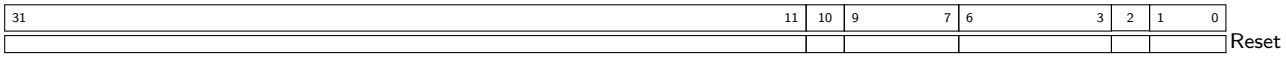
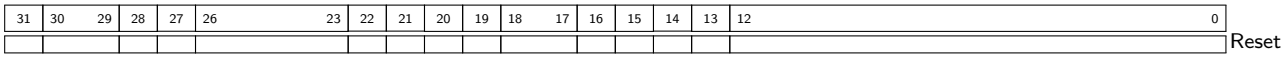
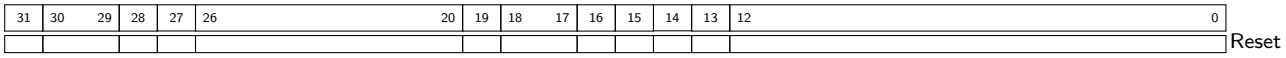
Reset


31
11
10
9
7
6
3
2
1
0
Reset


31
30
29
28
27
26
23
22
21
20
19
18
17
16
15
14
13
12
0
Reset


31
30
29
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26
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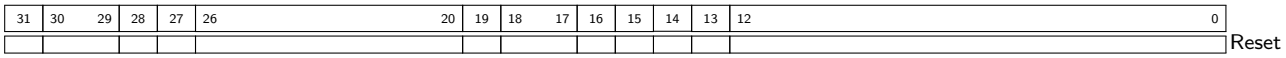
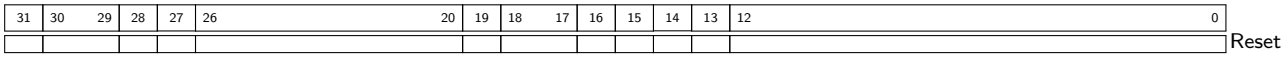
17
16
15
14
13
12
0
Reset


31
30
29
28
27
26
20
19
18
17
16
15
14
13
12
0
Reset


31
30
29
28
27
26
20
19
18
17
16
15
14
13
12
0
Reset

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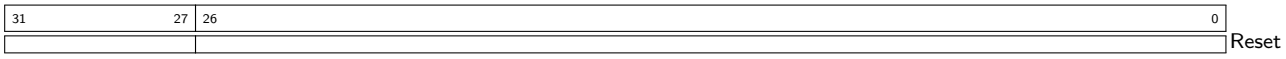
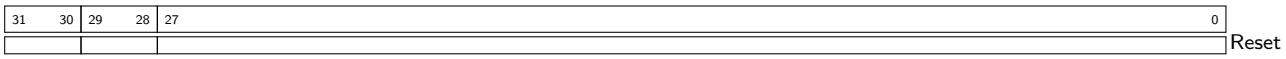
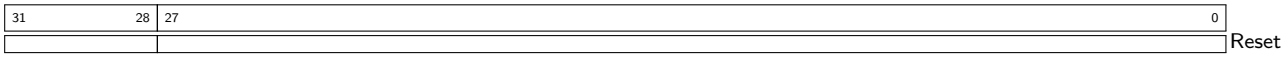
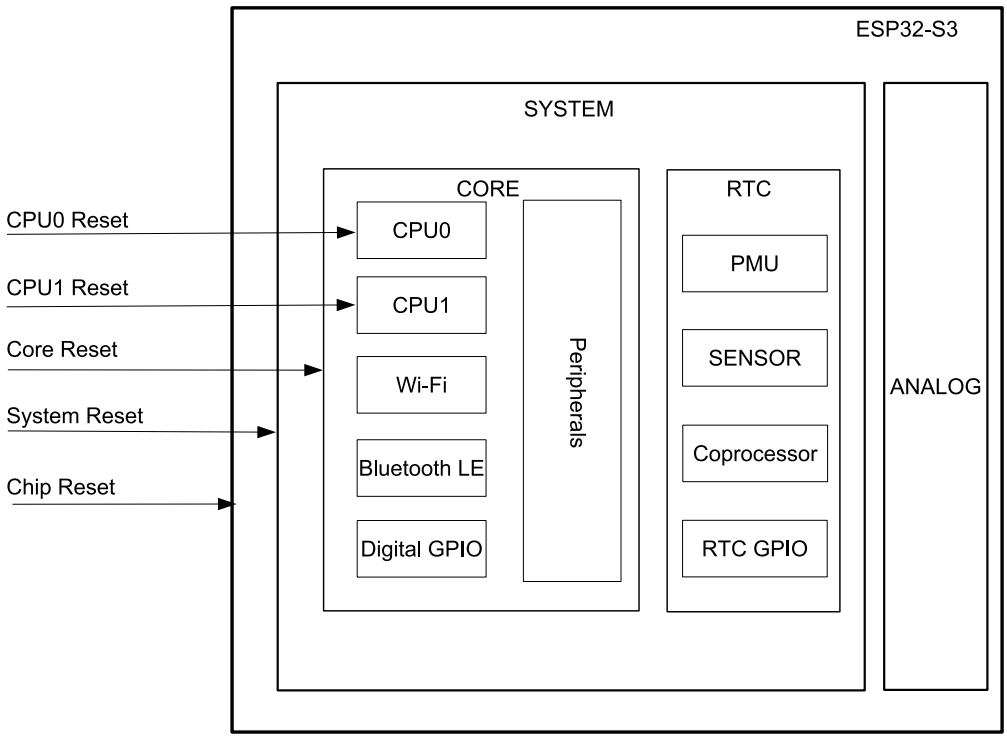
-


31
27
26
0
Reset


31
30
29
28
27
0
Reset


31
28
27
0
Reset


ESP32-S3
SYSTEM
CORE
CPU0
CPU1
Wi-Fi
Bluetooth LE
Digital GPIO
Peripherals
RTC
PMU
SENSOR
Coprocessor
RTC GPIO
ANALOG
CPU0 Reset
CPU1 Reset
Core Reset
System Reset
Chip Reset

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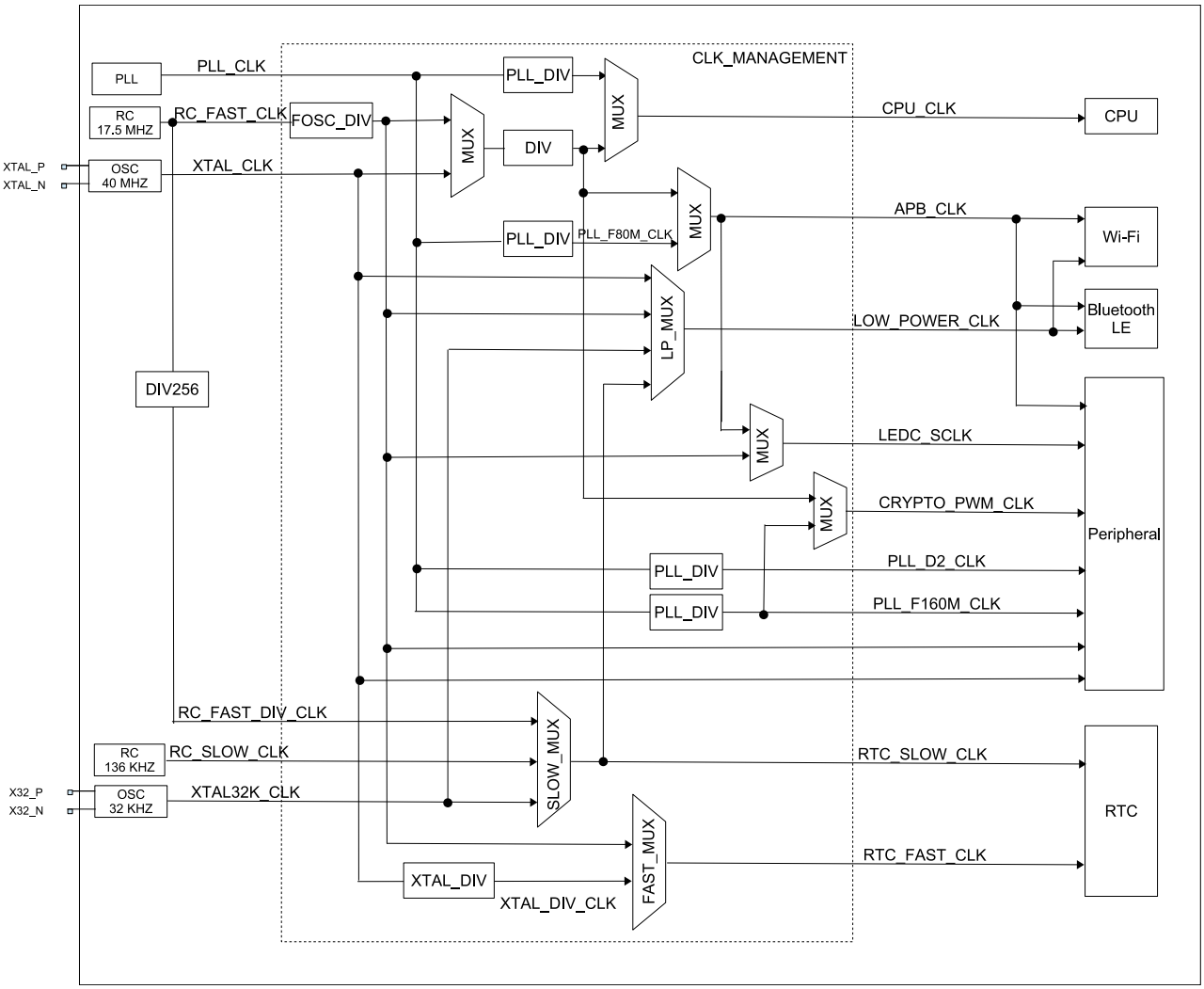
CLK_MANAGEMENT
PLL
PLL_CLK
RC
17.5 MHZ
RC_FAST_CLK
FOSC_DIV
XTAL_P
XTAL_N
OSC
40 MHZ
XTAL_CLK
MUX
PLL_DIV
DIV
MUX
CPU_CLK
CPU
MUX
APB_CLK
Wi-Fi
PLL_DIV
PLL_F80M_CLK
LP_MUX
LOW_POWER_CLK
Bluetooth
LE
DIV256
MUX
LEDC_SCLK
MUX
CRYPTO_PWM_CLK
Peripheral
PLL_DIV
PLL_D2_CLK
PLL_DIV
PLL_F160M_CLK
RC_FAST_DIV_CLK
RC
136 KHZ
RC_SLOW_CLK
SLOW_MUX
RTC_SLOW_CLK
X32_P
X32_N
OSC
32 KHZ
XTAL32K_CLK
RTC
FAST_MUX
RTC_FAST_CLK
XTAL_DIV
XTAL_DIV_CLK

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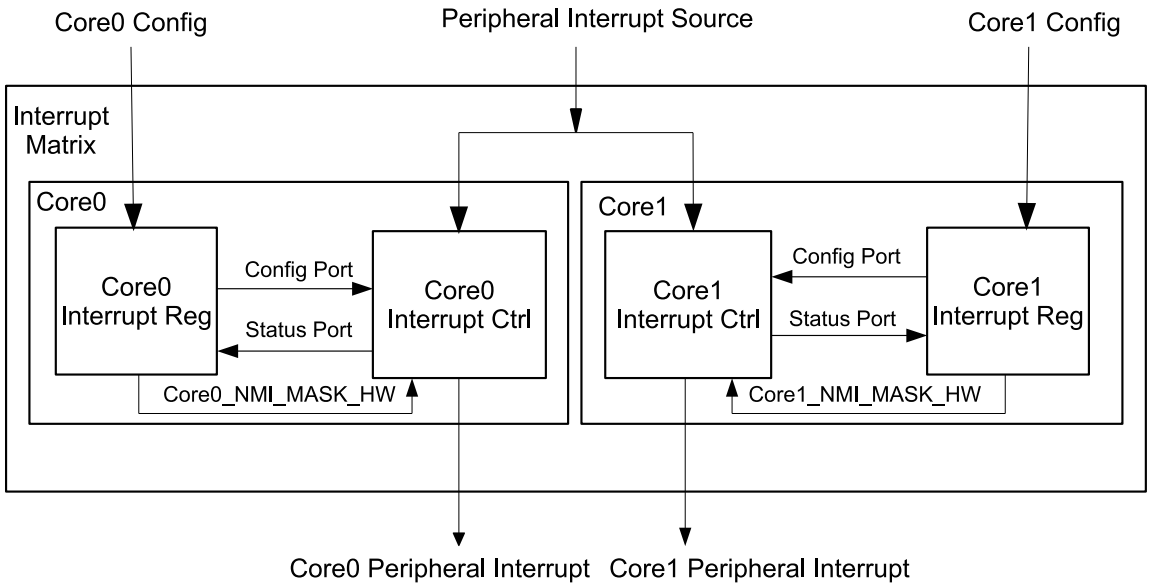
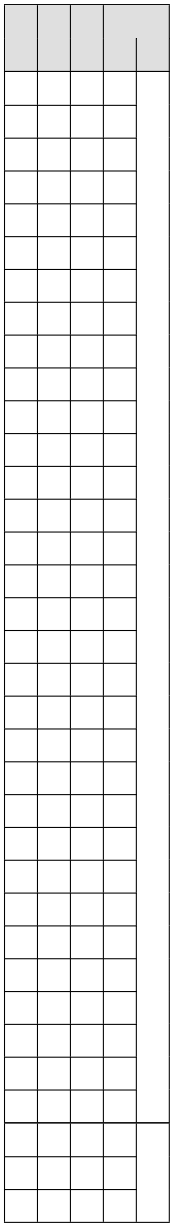
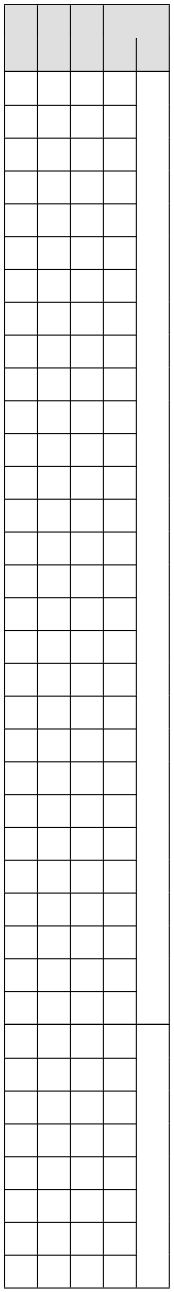
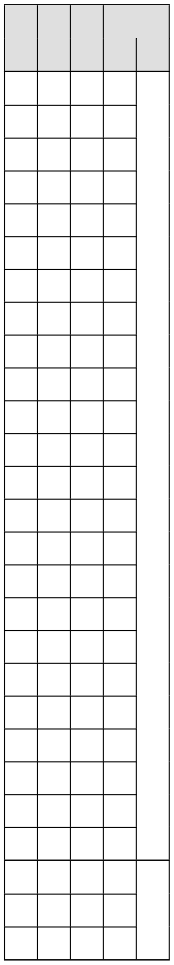

Core0 Config
Peripheral Interrupt Source
Core1 Config
Interrupt Matrix
Core0
Core0 Interrupt Reg
Config Port
Status Port
Core0 Interrupt Ctrl
Core0_NMI_MASK_HW
Core1
Core1 Interrupt Ctrl
Config Port
Status Port
Core1 Interrupt Reg
Core1_NMI_MASK_HW
Core0 Peripheral Interrupt
Core1 Peripheral Interrupt

-
-
-
-







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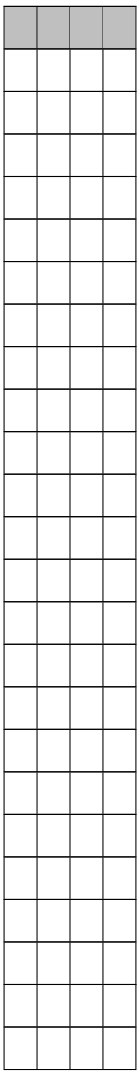

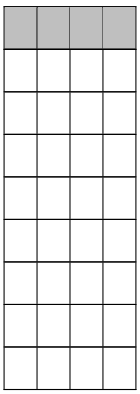

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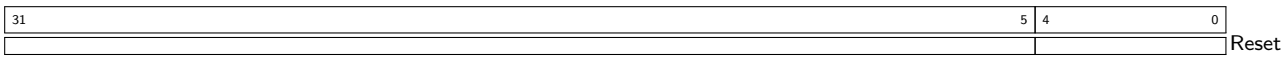
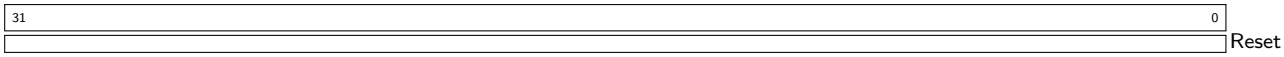
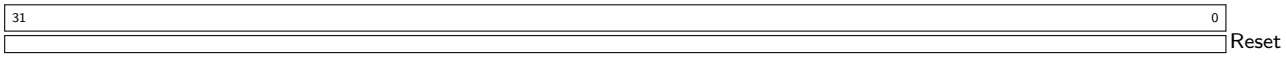
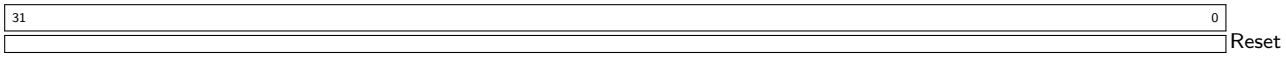
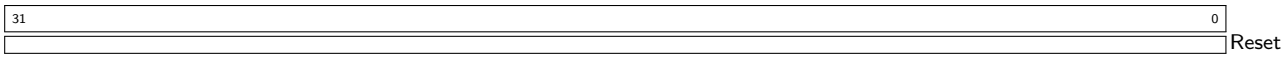
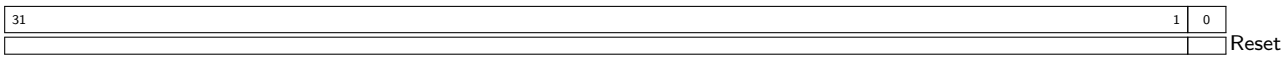

31
5
4
0
Reset

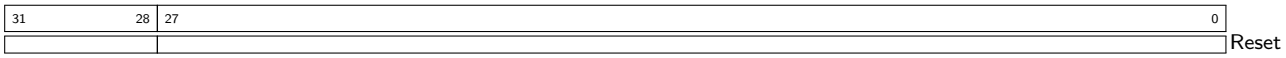

31
0
Reset

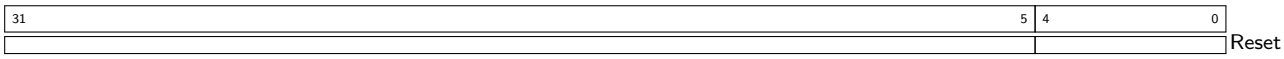

31
0
Reset

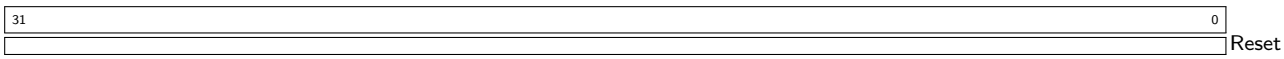

31
0
Reset

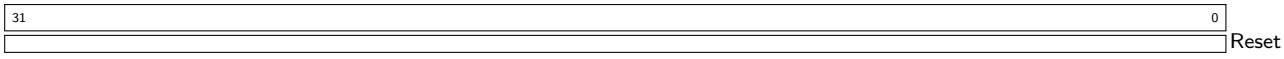

31
0
Reset


31
1
0
Reset


31
28
27
0
Reset


31
5
4
0
Reset


31
0
Reset


31
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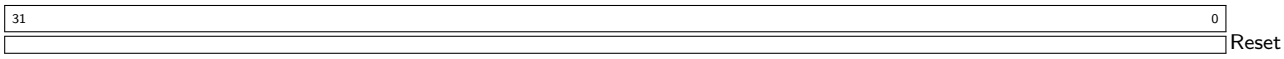
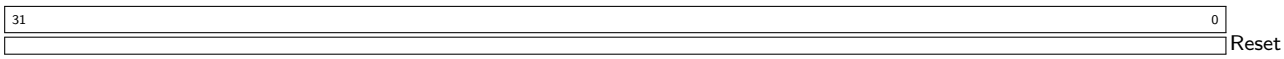
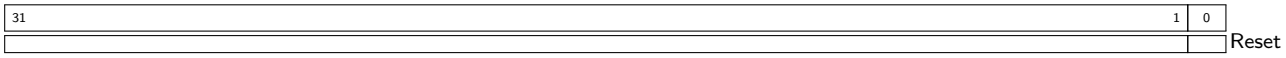
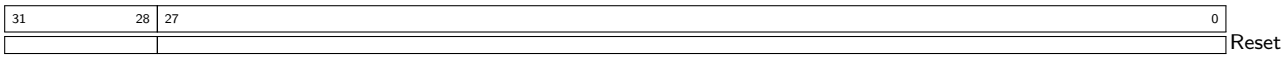
Reset


31
0
Reset


31
0
Reset


31
1
0
Reset


31
28
27
0
Reset

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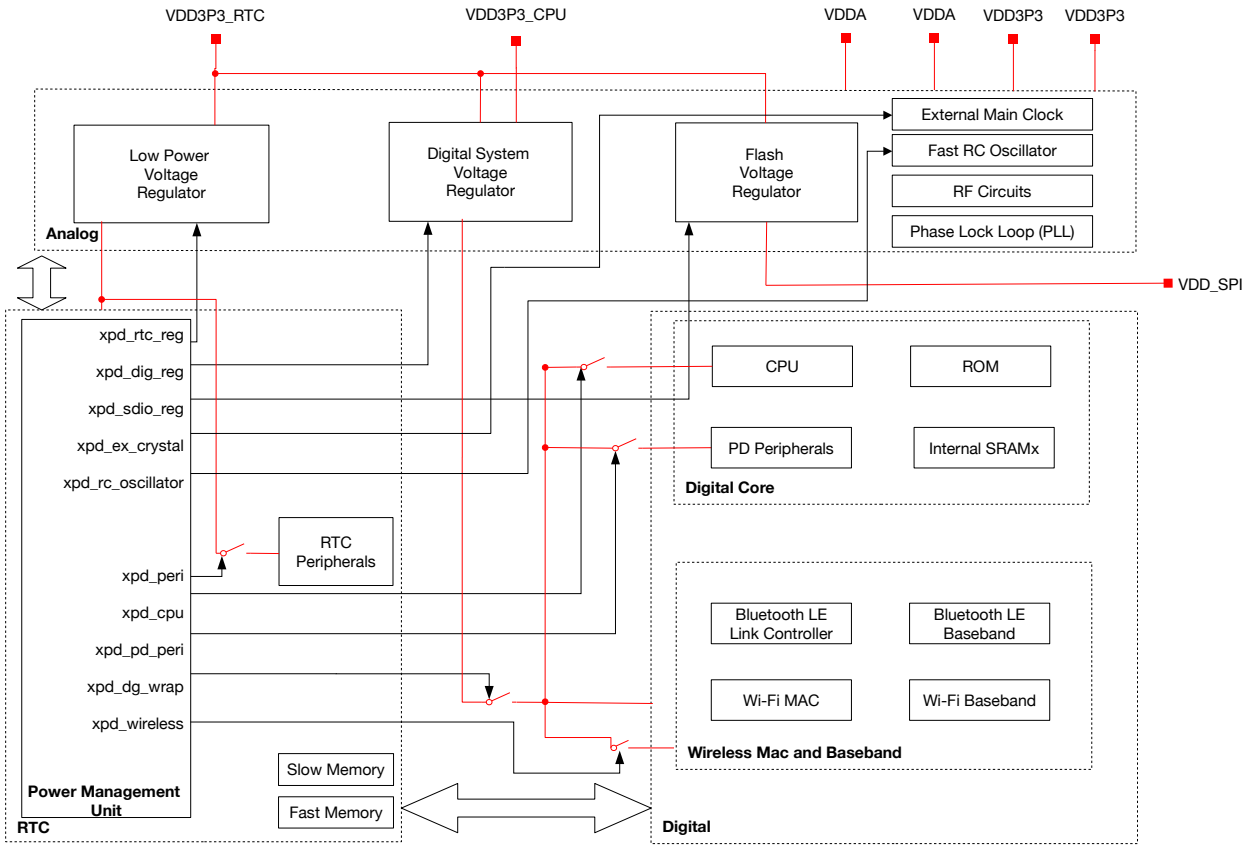
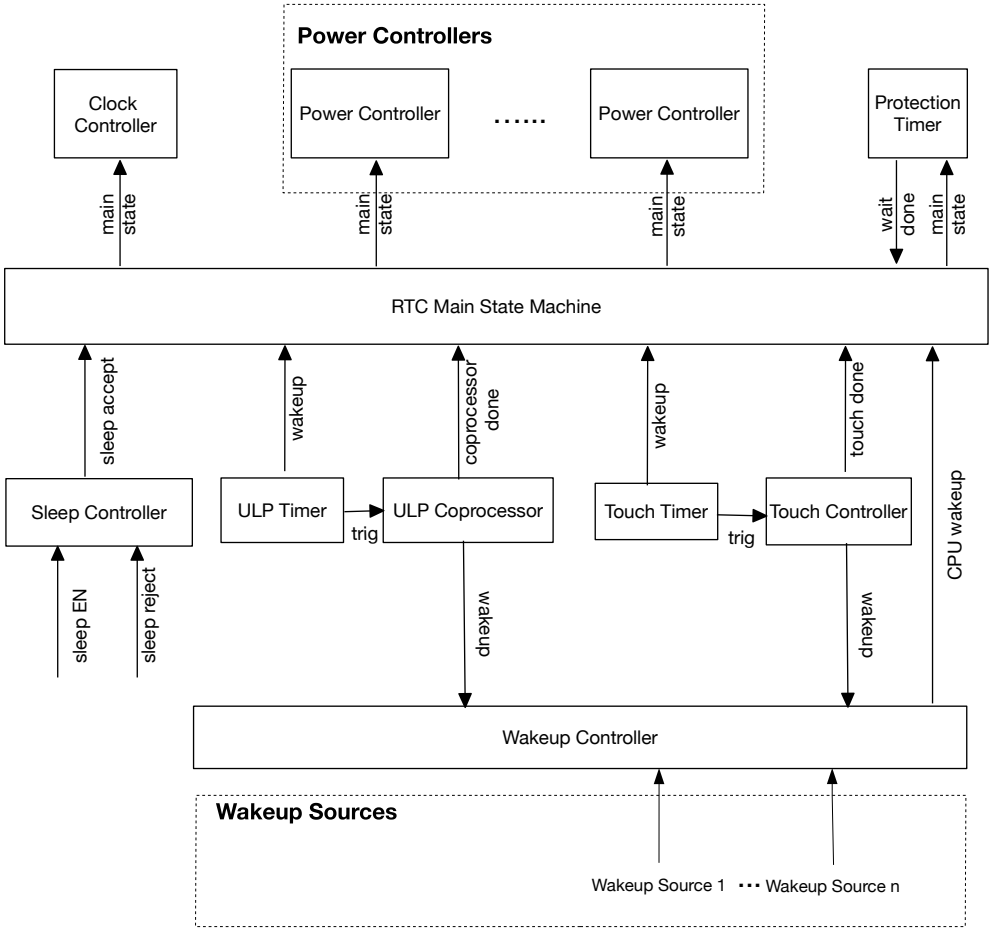
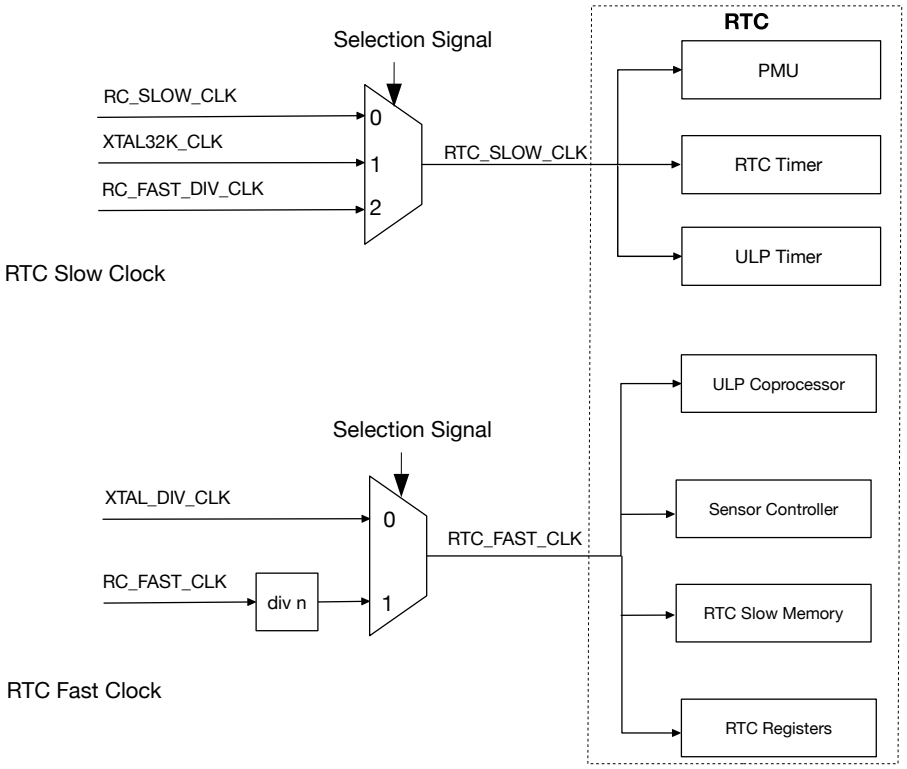
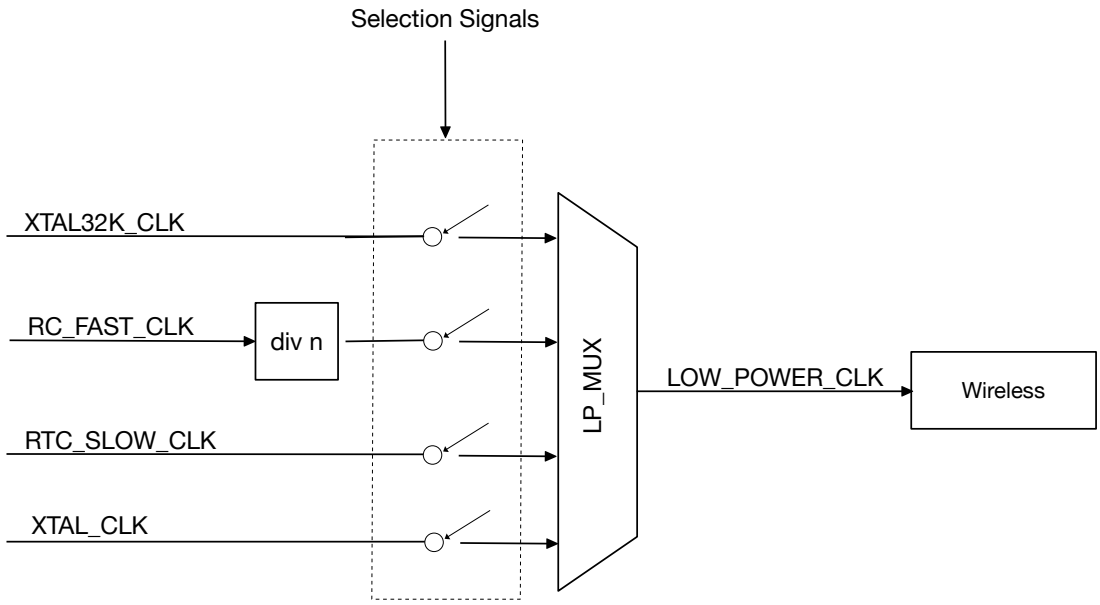


Red lines represent power distribution


Power Controllers
Clock Controller
Power Controller
.....
Power Controller
Protection Timer
main state
main state
main state
wait done
main state
RTC Main State Machine
sleep accept
wakeup
coprocessor done
wakeup
touch done
CPU wakeup
Sleep Controller
ULP Timer
trig
ULP Coprocessor
Touch Timer
trig
Touch Controller
sleep EN
sleep reject
wakeup
wakeup
Wakeup Controller
Wakeup Sources
Wakeup Source 1
Wakeup Source n


RTC
Selection Signal
RC_SLOW_CLK
XTAL32K_CLK
RC_FAST_DIV_CLK
0
1
2
RTC_SLOW_CLK
PMU
RTC Timer
ULP Timer
RTC Slow Clock
ULP Coprocessor
Selection Signal
XTAL_DIV_CLK
RC_FAST_CLK
div n
0
1
RTC_FAST_CLK
Sensor Controller
RTC Slow Memory
RTC Fast Clock
RTC Registers


Selection Signals
XTAL32K_CLK
RC_FAST_CLK
div n
RTC_SLOW_CLK
XTAL_CLK
LP_MUX
LOW_POWER_CLK
Wireless

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-
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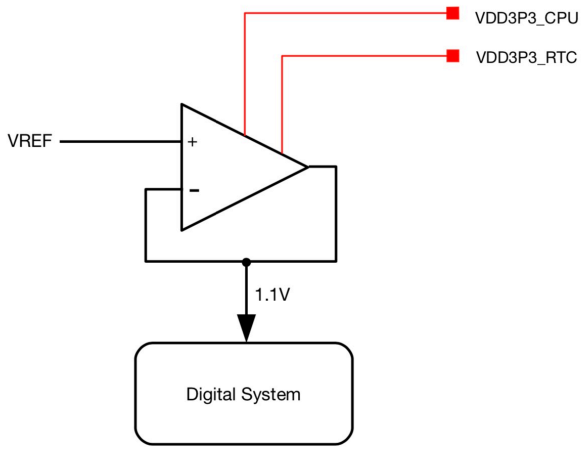
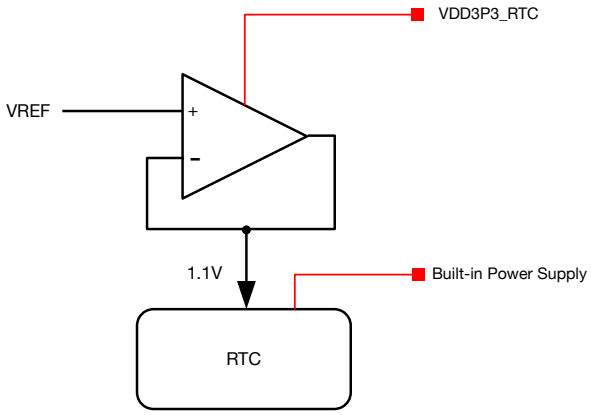
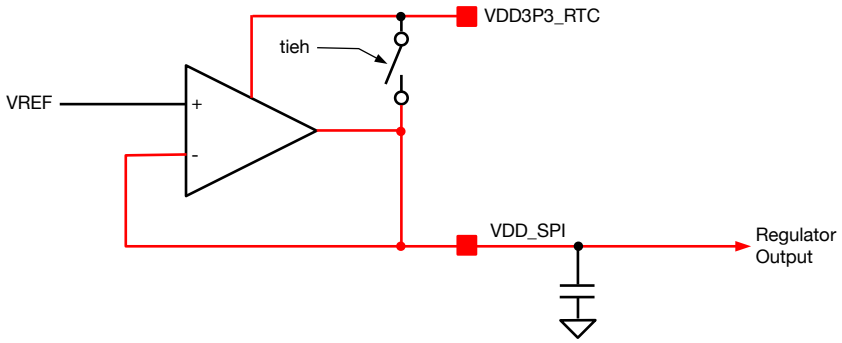
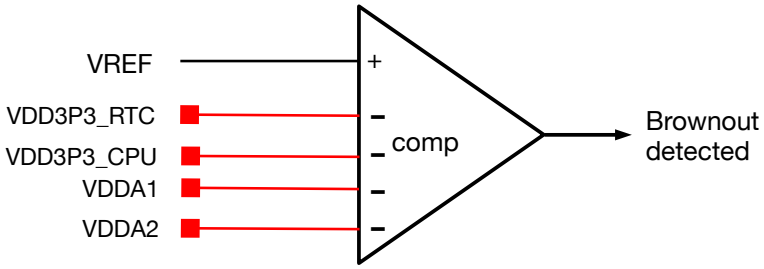

VDD3P3_CPU
VDD3P3_RTC
VREF
+
-
1.1V
Digital System


VDD3P3_RTC
VREF
+
-
1.1V
Built-in Power Supply
RTC

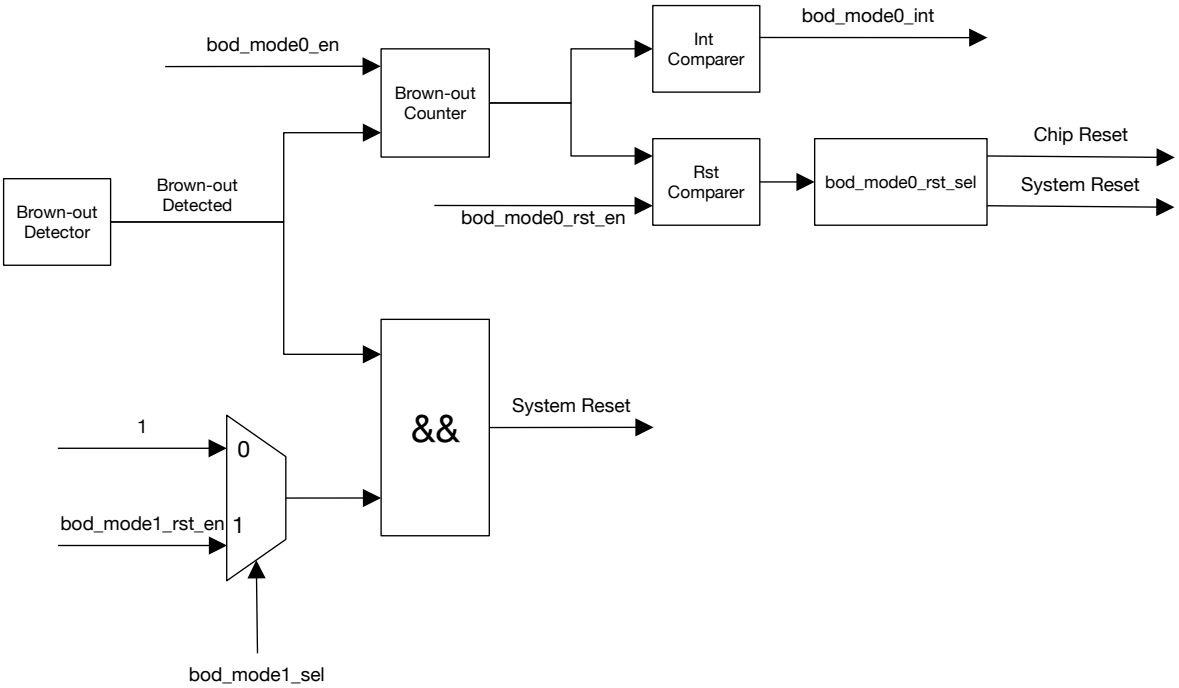

VDD3P3_RTC
tieh
VREF
+
-
VDD_SPI
Regulator
Output

-
-
-
-
-

-


VREF
VDD3P3_RTC
VDD3P3_CPU
VDDA1
VDDA2
+
comp
Brownout
detected

-
-


bod_mode0_en
Brown-out Counter
Int Comparer
bod_mode0_int
Brown-out Detector
Brown-out Detected
Rst Comparer
bod_mode0_rst_en
bod_mode0_rst_sel
Chip Reset
System Reset
&&
System Reset
1
0
bod_mode1_rst_en
1
bod_mode1_sel

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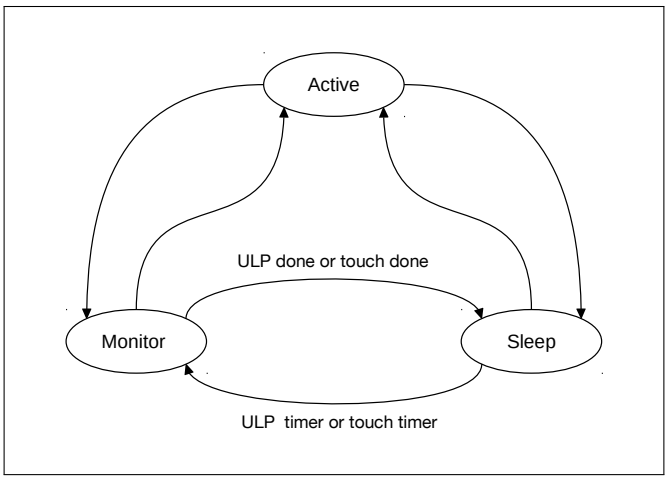
-
-
-
-
-
-


Active
ULP done or touch done
Monitor
Sleep
ULP timer or touch timer

123

	10			

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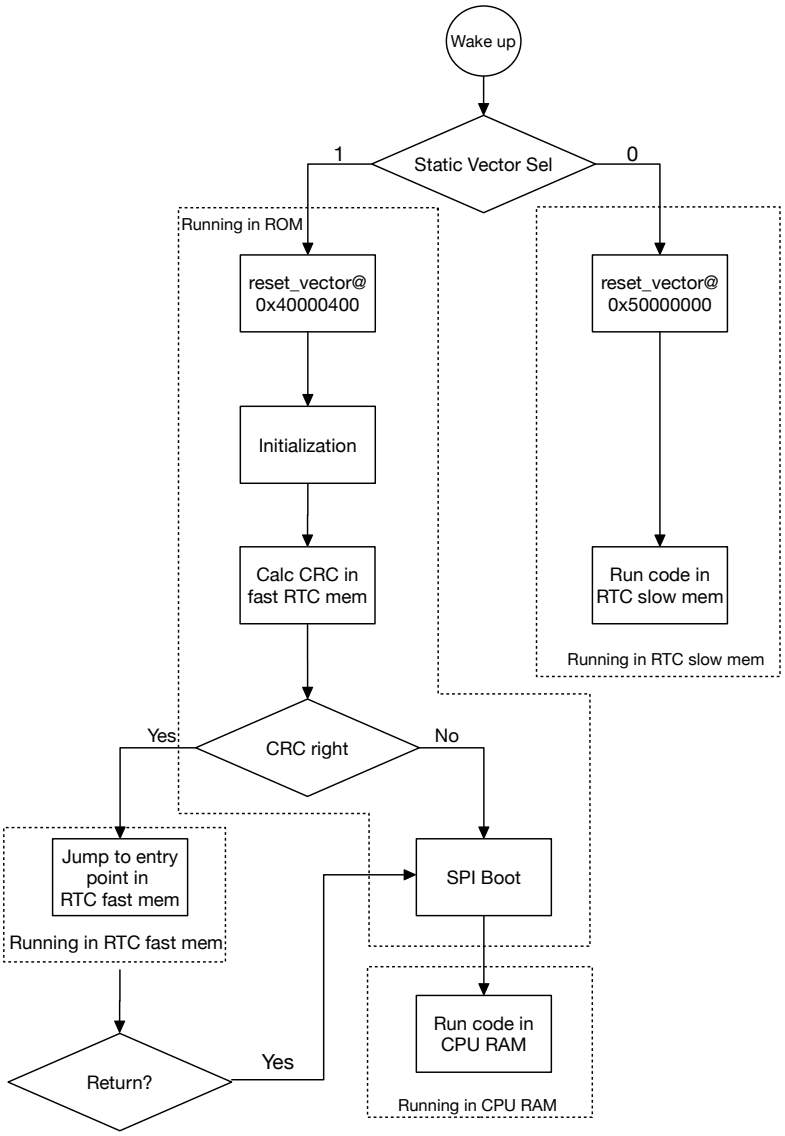
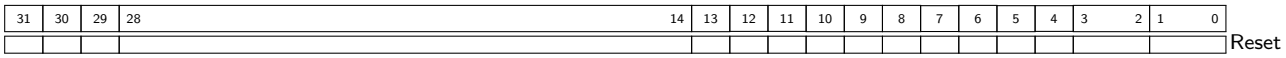

Wake up
Static Vector Sel
1
0
Running in ROM
reset_vector@
0x40000400
Initialization
Calc CRC in
fast RTC mem
reset_vector@
0x50000000
Run code in
RTC slow mem
Running in RTC slow mem
Yes
CRC right
No
Jump to entry
point in
RTC fast mem
Running in RTC fast mem
SPI Boot
Run code in
CPU RAM
Running in CPU RAM
Return?
Yes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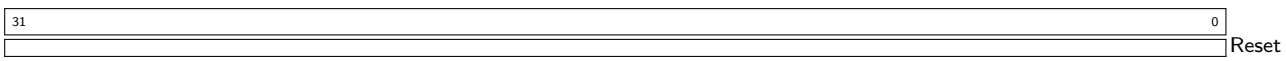
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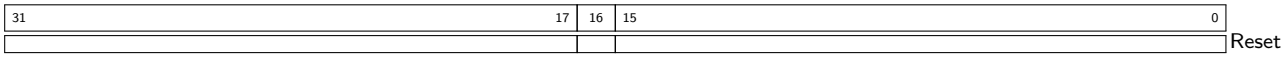
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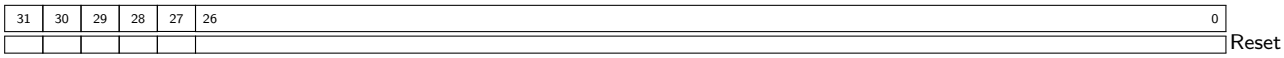
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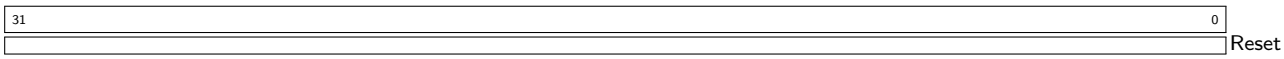
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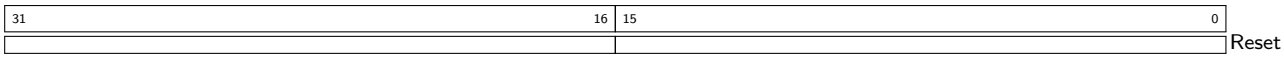
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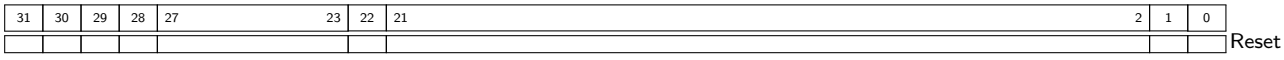
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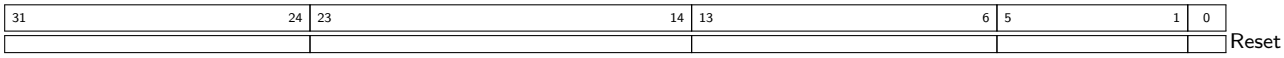
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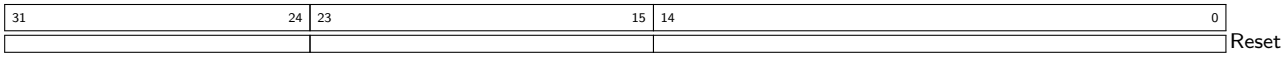
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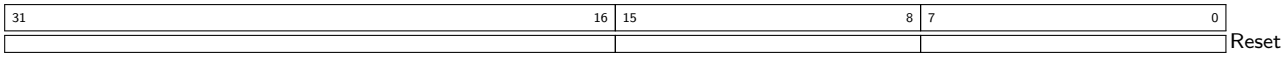
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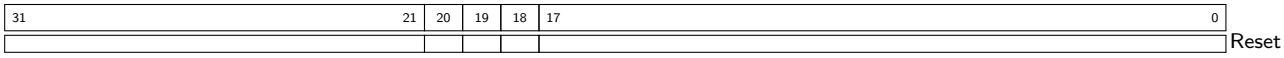
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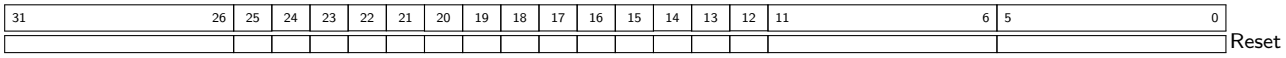
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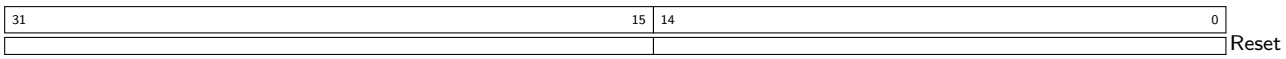
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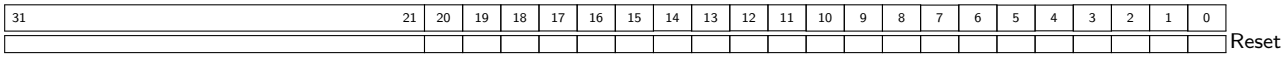
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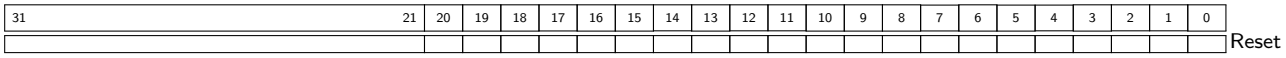
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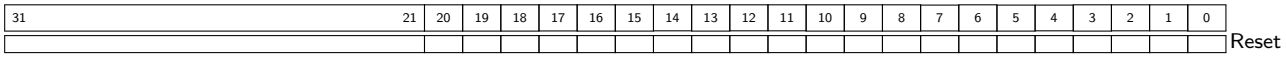
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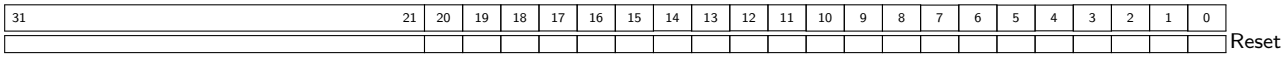
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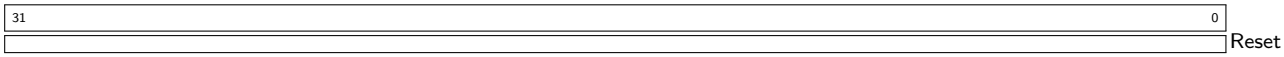
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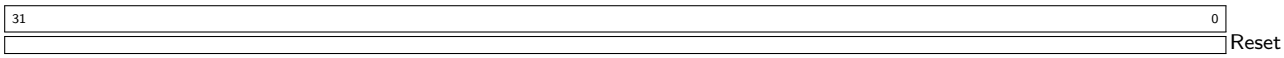
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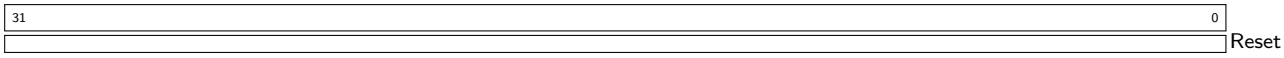
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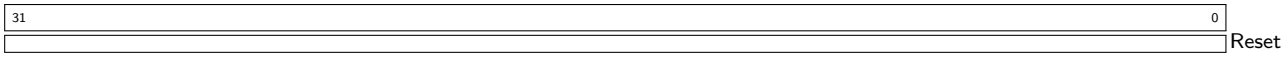
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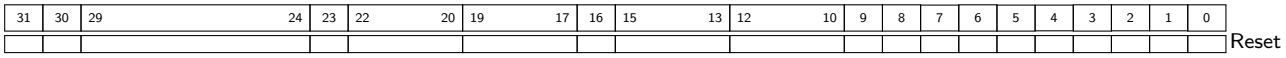
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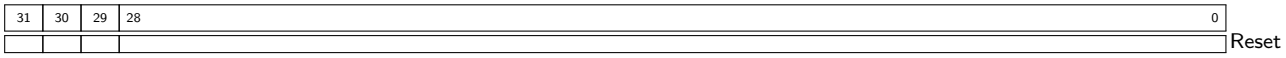
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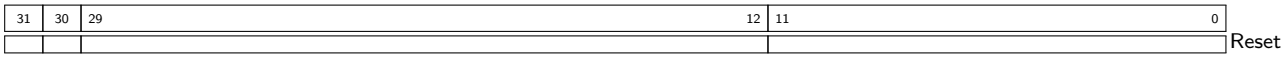
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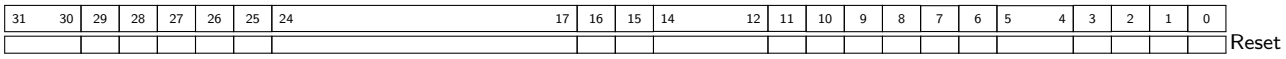
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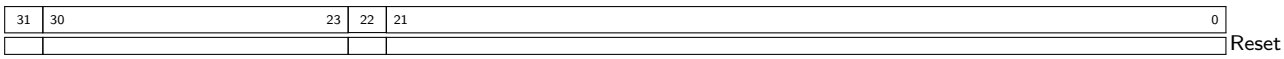
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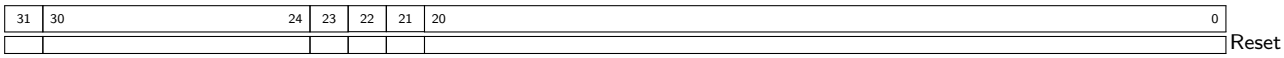
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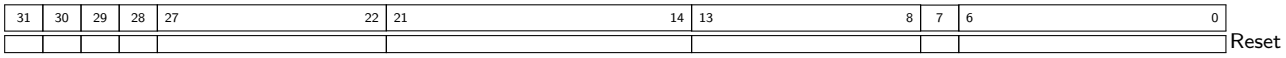
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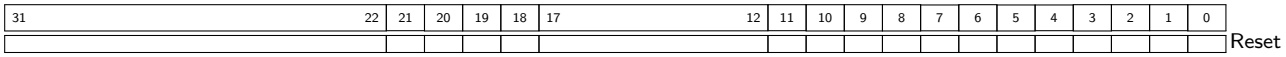
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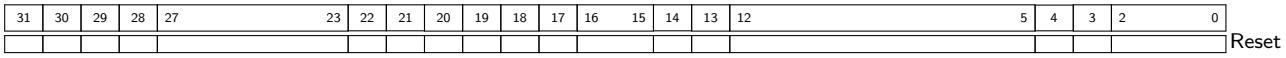
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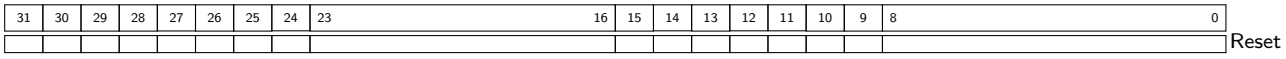
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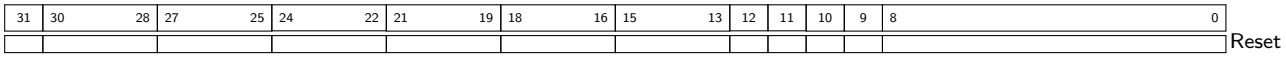
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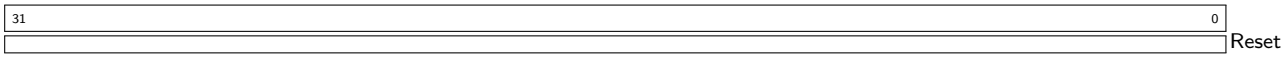
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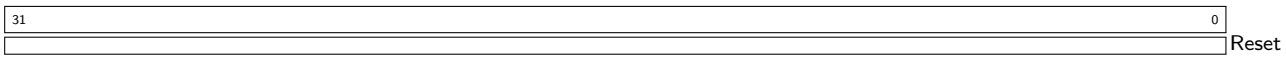
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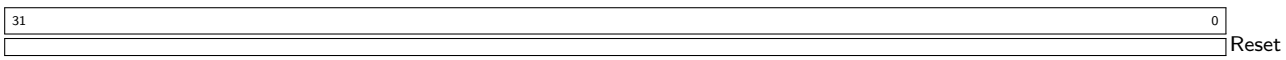
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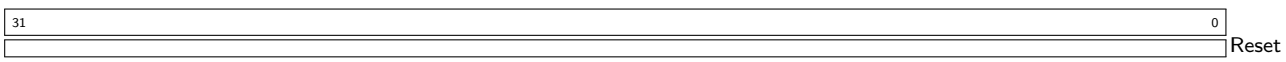
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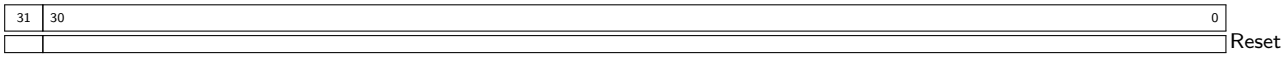
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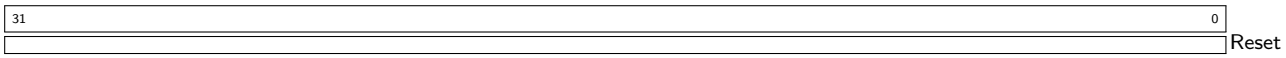
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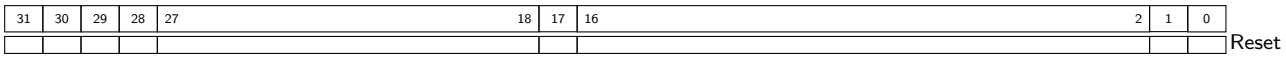
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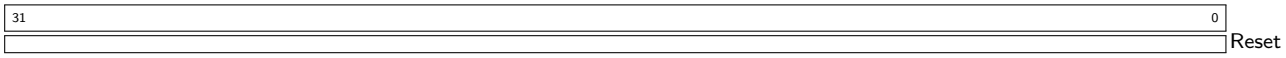
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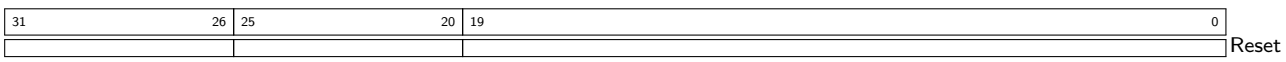
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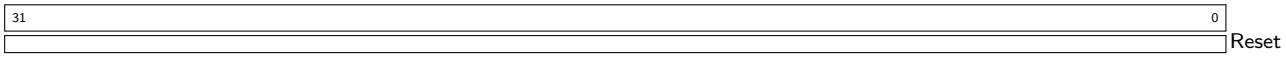
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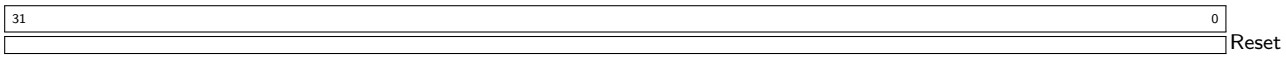
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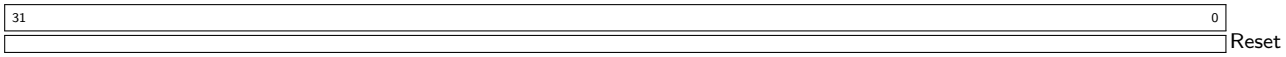
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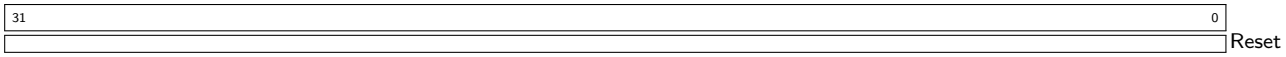
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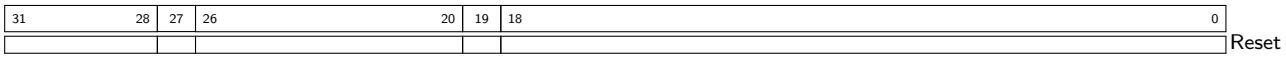
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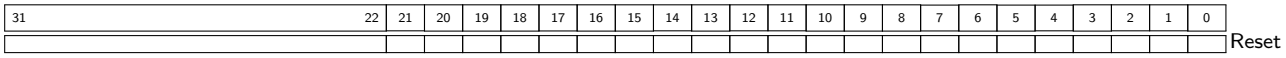
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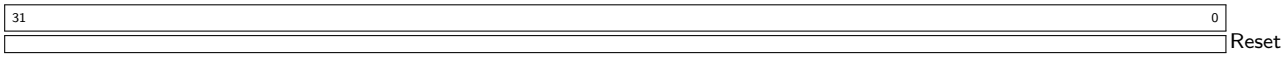
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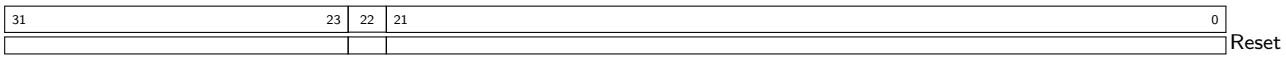
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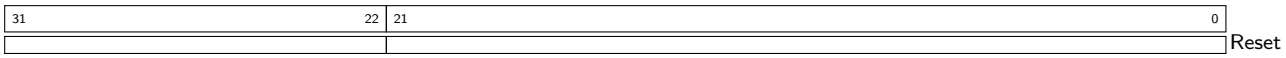
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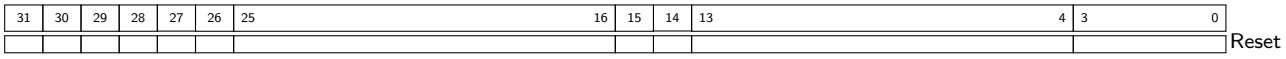
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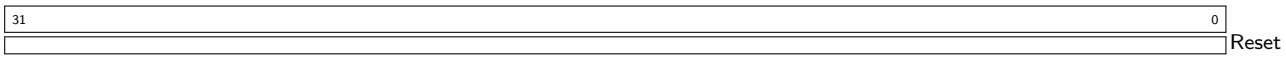
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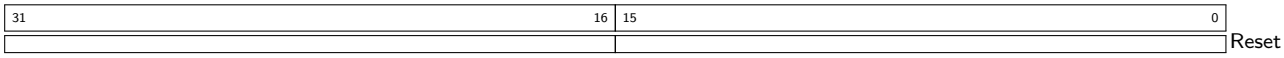
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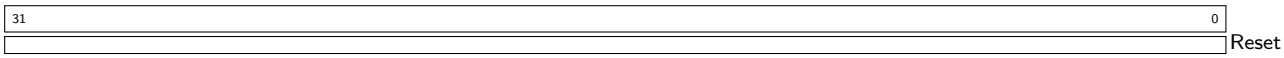
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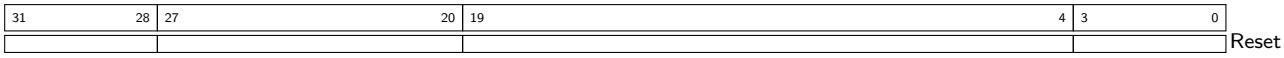
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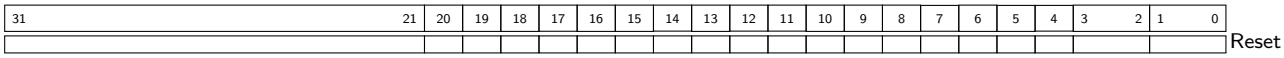
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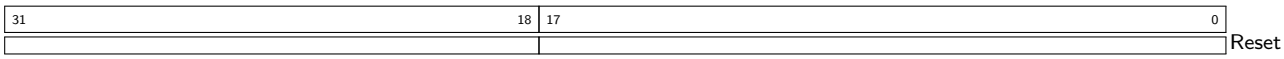
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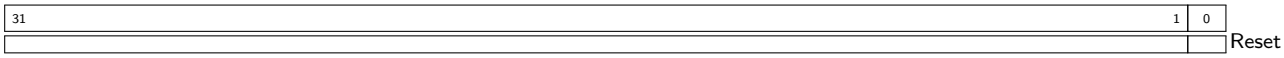
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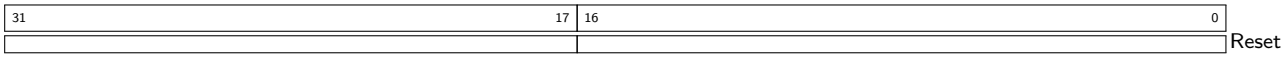
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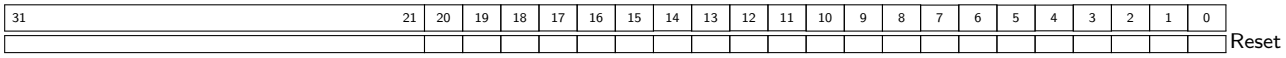
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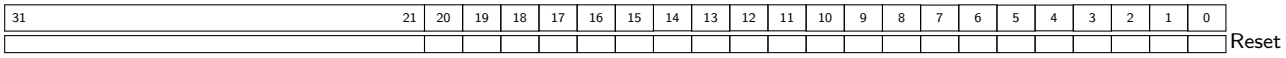
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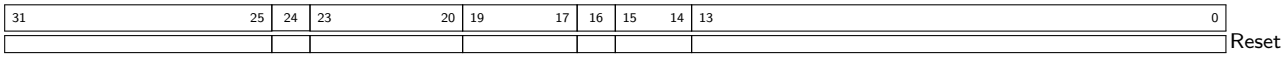
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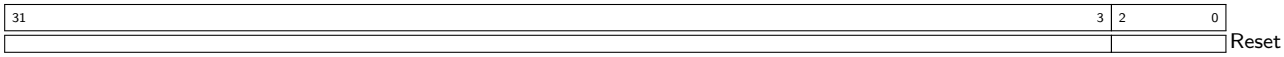
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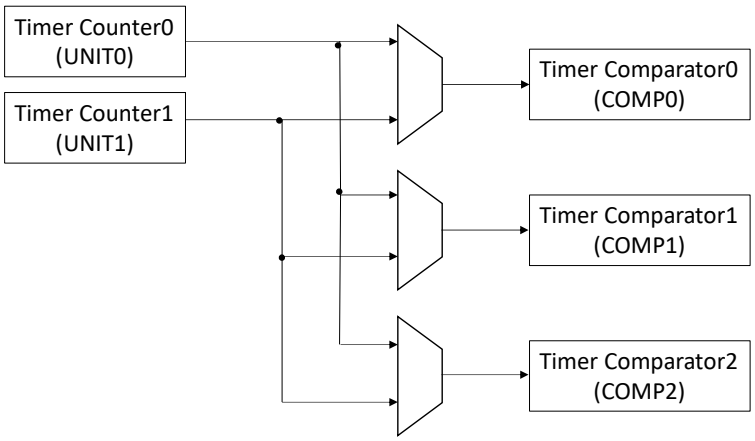

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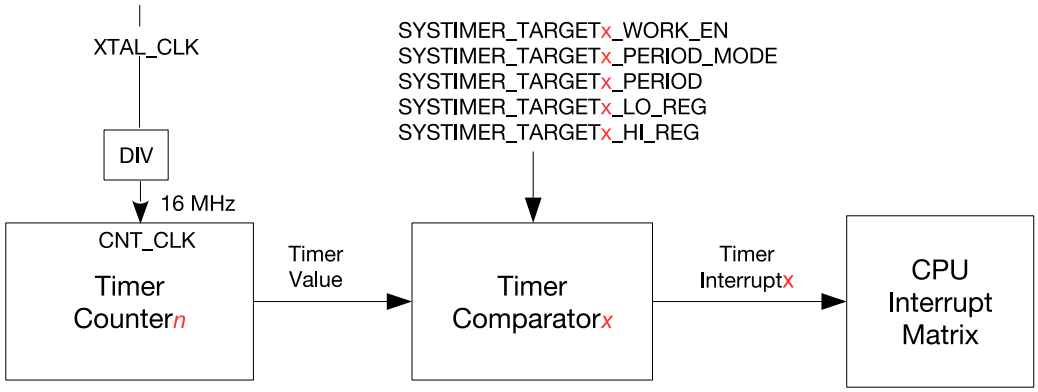

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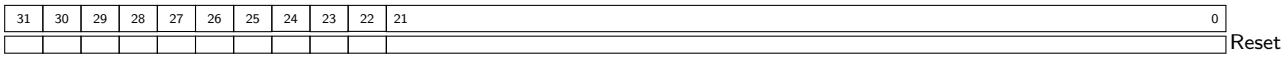
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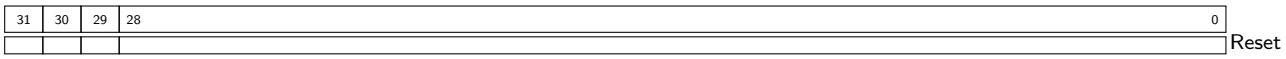
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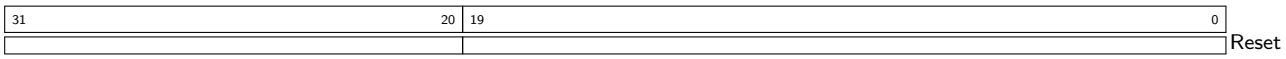
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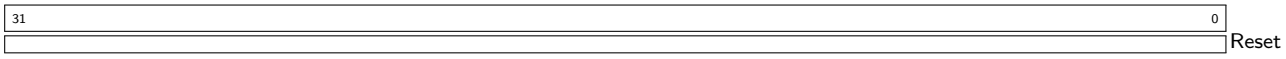
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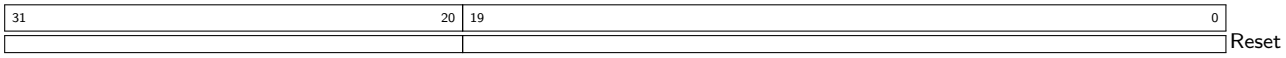
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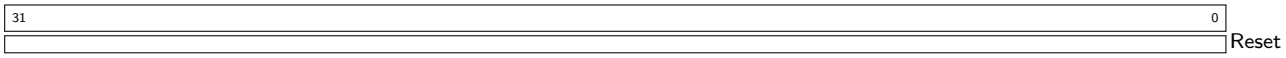
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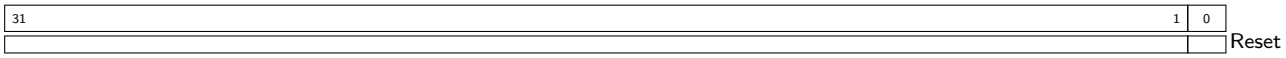
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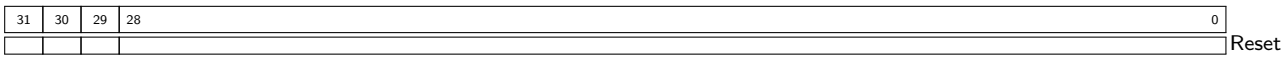
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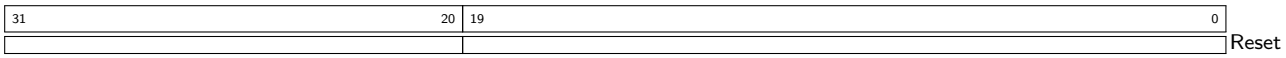
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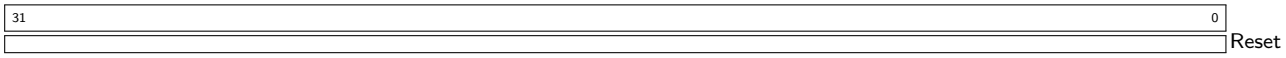
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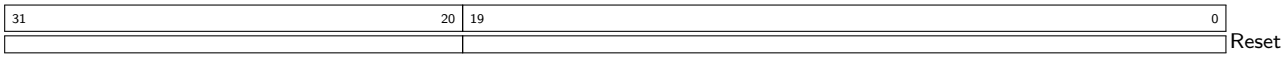
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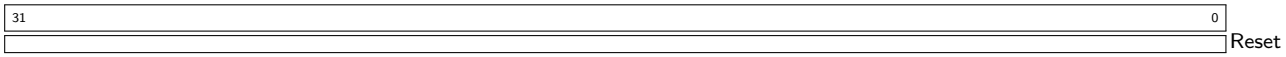
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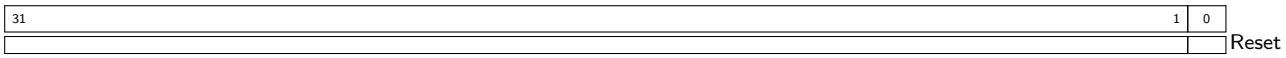
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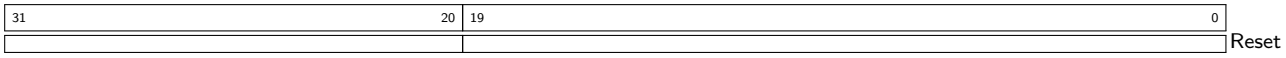
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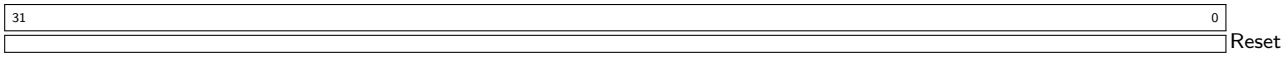
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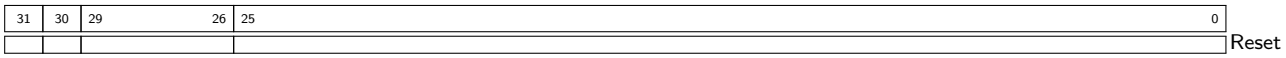
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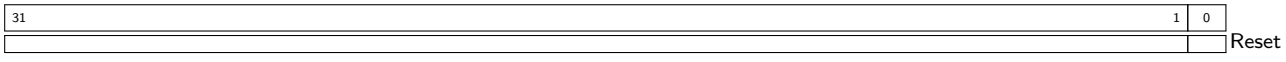
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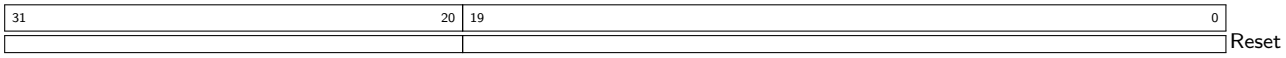
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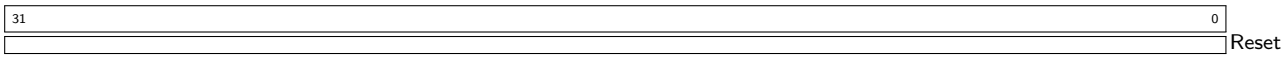
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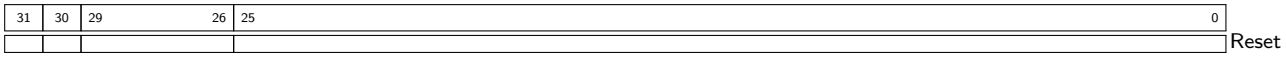
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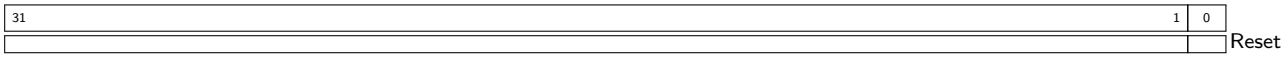
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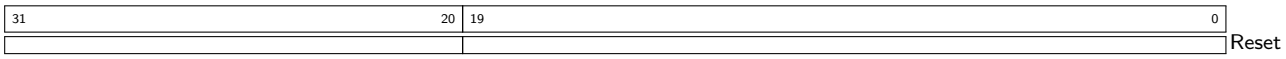
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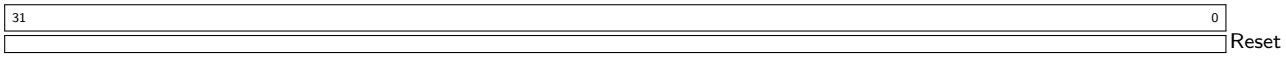
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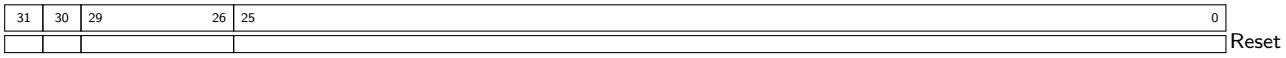
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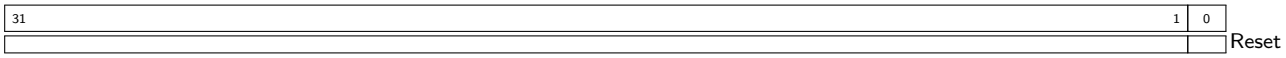
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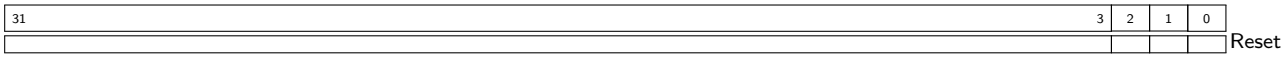
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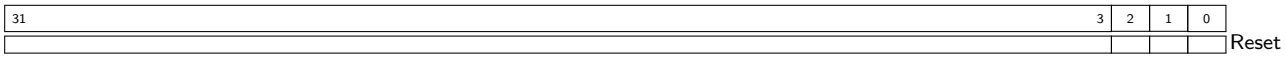
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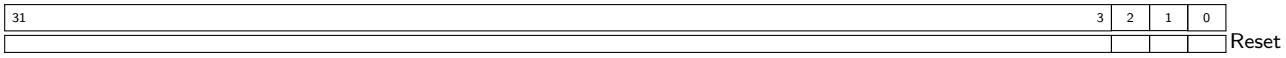
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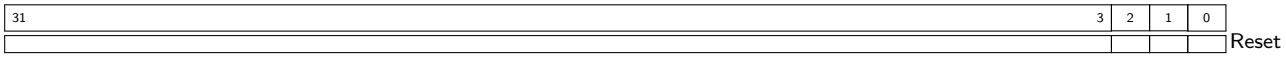
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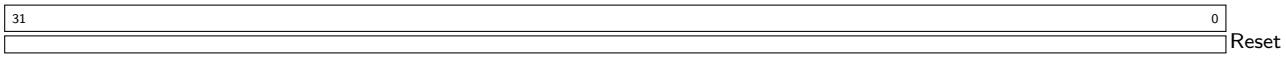
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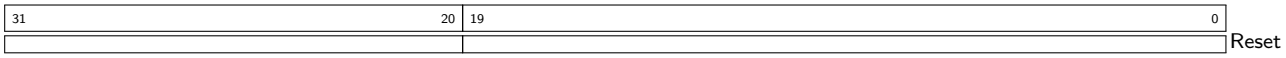
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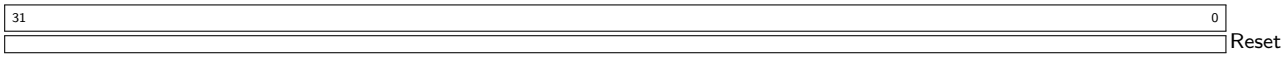
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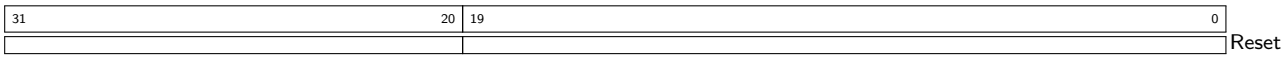
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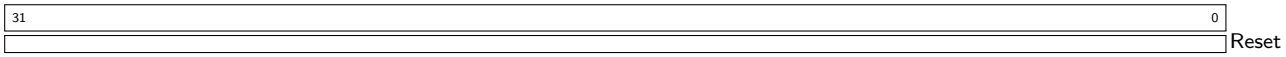
31
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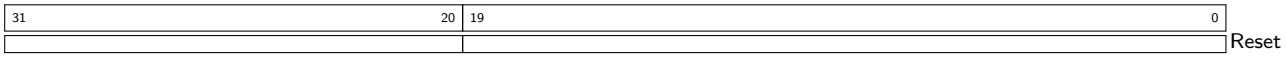
Reset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19
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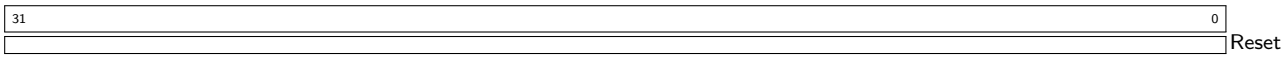
Reset


31
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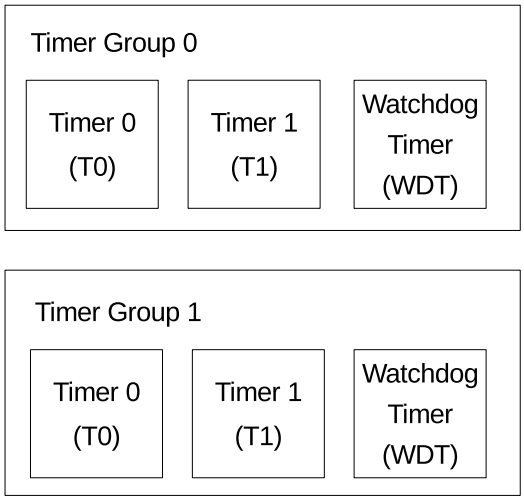
Reset


Timer Group 0
Timer 0
(T0)
Timer 1
(T1)
Watchdog
Timer
(WDT)
Timer Group 1
Timer 0
(T0)
Timer 1
(T1)
Watchdog
Timer
(WDT)

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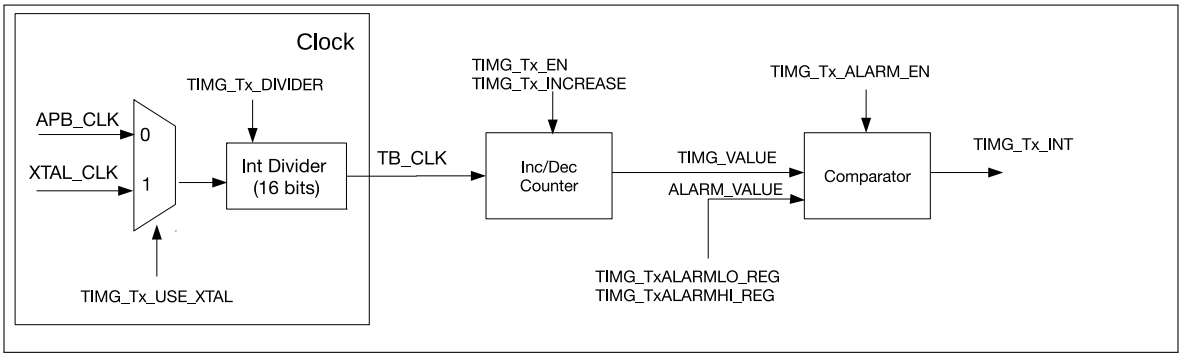

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	$->2^{53}$	
	$<-\leq 2^{53}$	
	$\leq-<2^{53}$	
	$-\geq 2^{53}$	

	$->2^{53}$	
	$<-\leq 2^{53}$	
	$\leq -<2^{53}$	
	$-\geq 2^{53}$	

$$frtc = \frac{C0 \times fXTALCLK}{C1}$$

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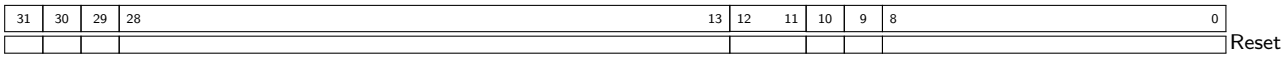
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9
8
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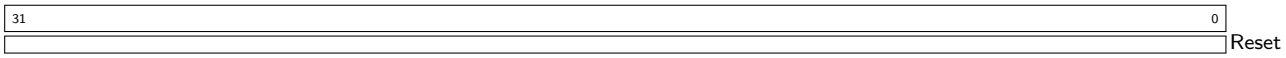
Reset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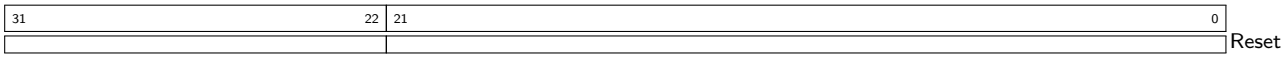
Reset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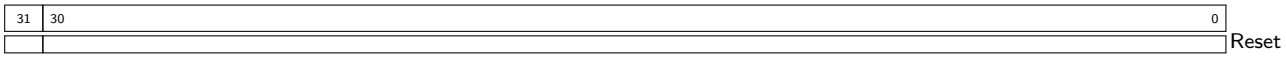
Reset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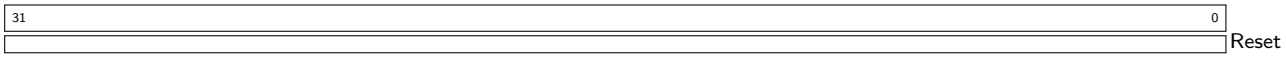
30
0
Reset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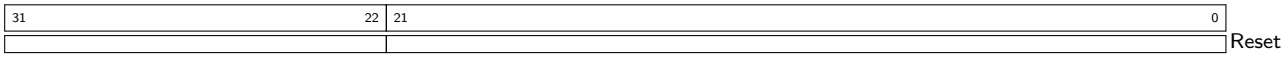
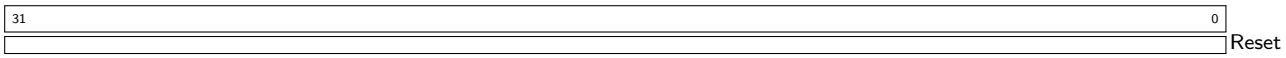
Reset


31
22
21
0
Reset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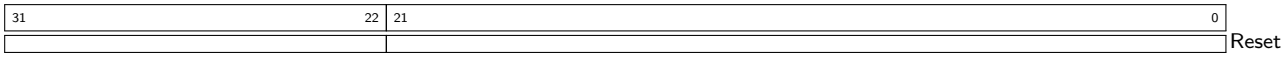
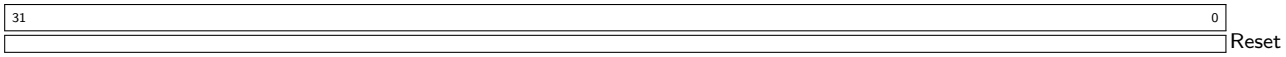
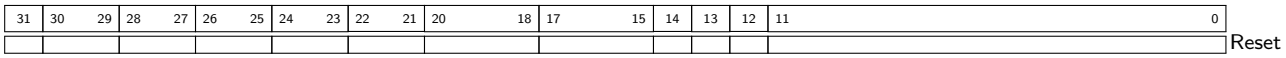
Reset


31
22
21
0
Reset


31
0
Reset


31
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21
20
18
17
15
14
13
12
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0
Reset

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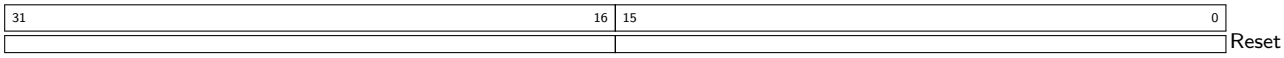
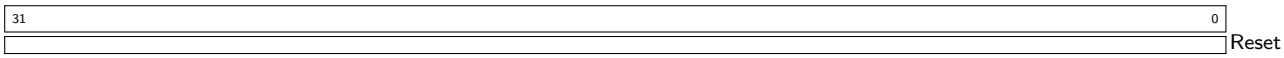

31
16
15
0
Reset


31
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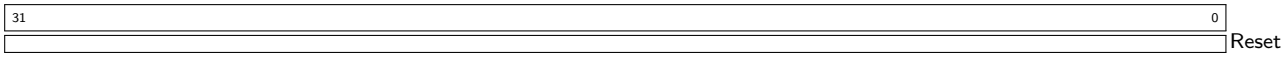
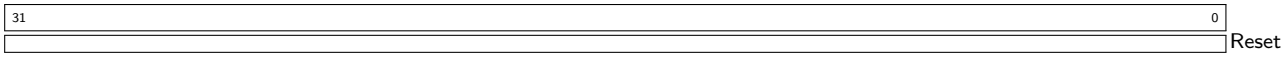
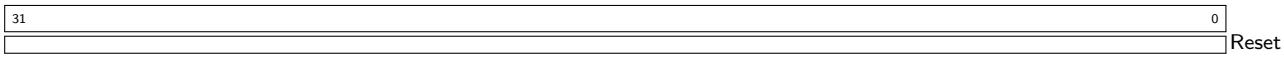
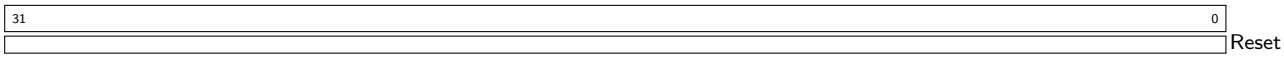
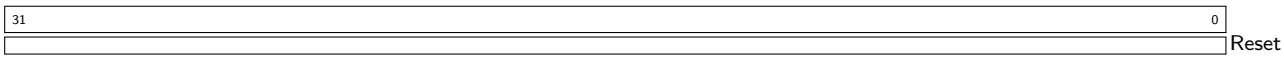
Reset

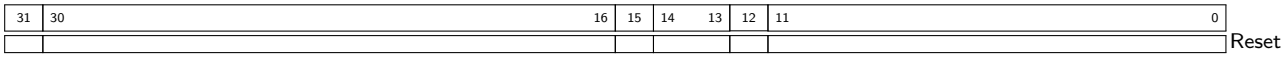

31
0
Reset

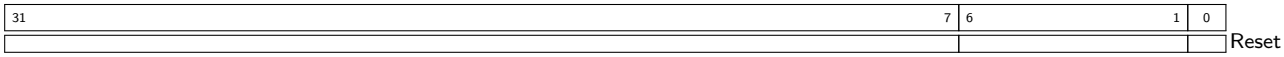

31
0
Reset

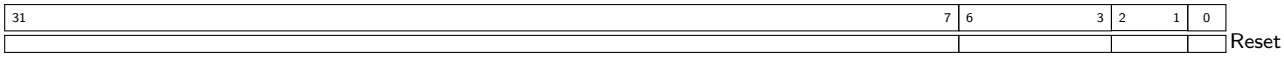

31
0
Reset

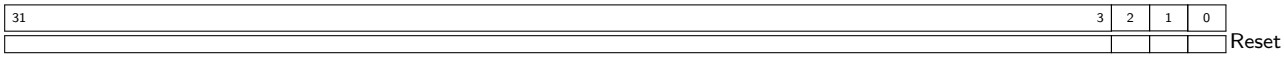

31
0
Reset

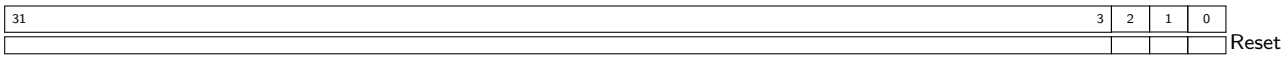

31
0
Reset

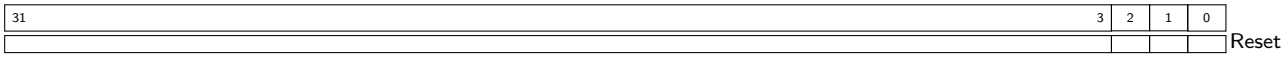

31
30
16
15
14
13
12
11
0
Reset

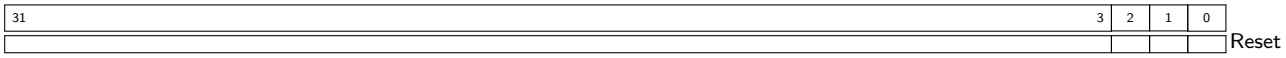

31
7
6
1
0
Reset

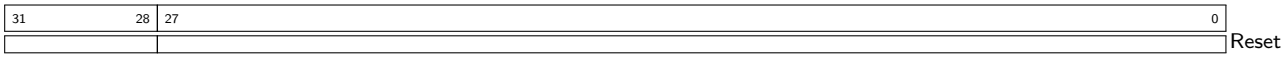

31
7
6
3
2
1
0
Reset

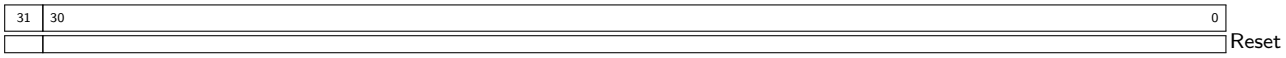

31
3
2
1
0
Reset

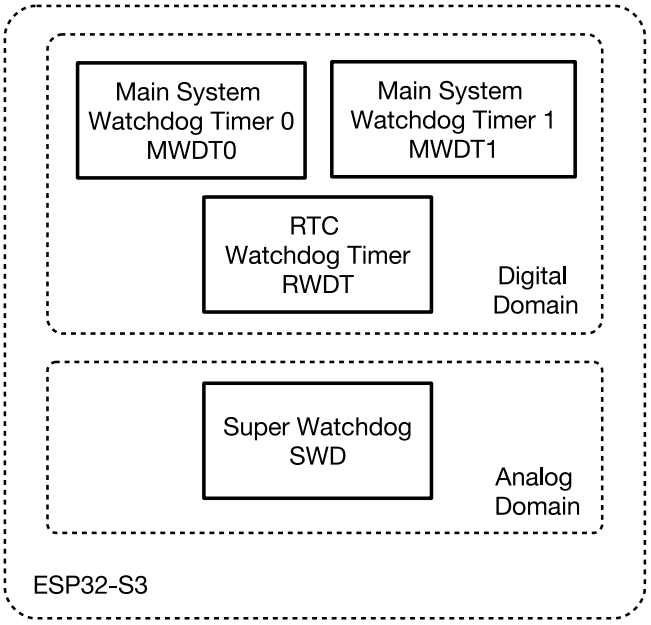

31
3
2
1
0
Reset


31
3
2
1
0
Reset


31
3
2
1
0
Reset


31
28
27
0
Reset


31
30
0
Reset


Main System
Watchdog Timer 0
MWDT0
Main System
Watchdog Timer 1
MWDT1
RTC
Watchdog Timer
RWDT
Digital
Domain
Super Watchdog
SWD
Analog
Domain
ESP32-S3

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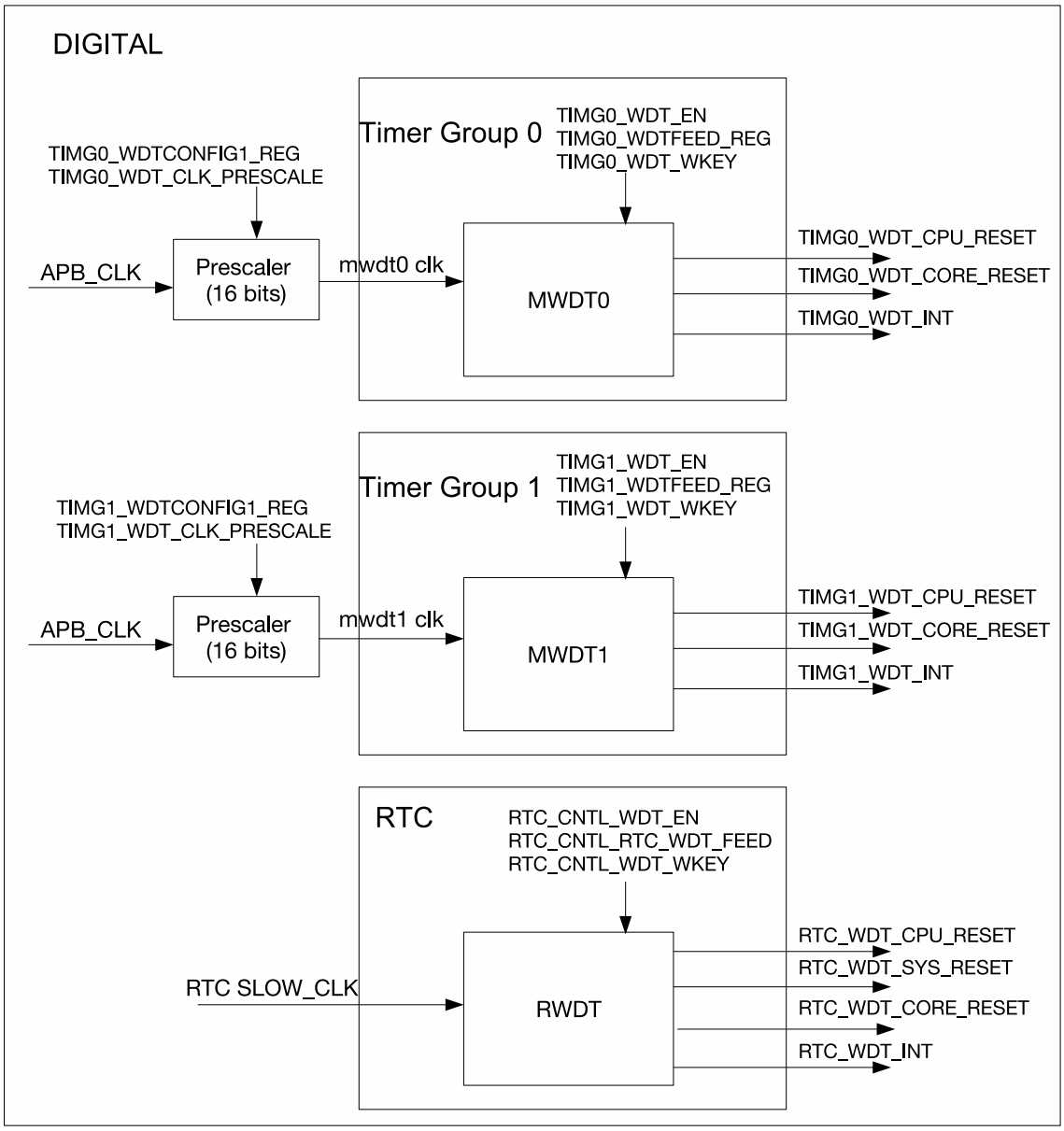
DIGITAL
Timer Group 0
TIMG0_WDT_EN
TIMG0_WDTFEED_REG
TIMG0_WDT_WKEY
TIMG0_WDTCONFIG1_REG
TIMG0_WDT_CLK_PRESCALE
APB_CLK
Prescaler
(16 bits)
mwdt0 clk
MWDT0
TIMG0_WDT_CPU_RESET
TIMG0_WDT_CORE_RESET
TIMG0_WDT_INT
Timer Group 1
TIMG1_WDT_EN
TIMG1_WDTFEED_REG
TIMG1_WDT_WKEY
TIMG1_WDTCONFIG1_REG
TIMG1_WDT_CLK_PRESCALE
APB_CLK
Prescaler
(16 bits)
mwdt1 clk
MWDT1
TIMG1_WDT_CPU_RESET
TIMG1_WDT_CORE_RESET
TIMG1_WDT_INT
RTC
RTC_CNTL_WDT_EN
RTC_CNTL_RTC_WDT_FEED
RTC_CNTL_WDT_WKEY
RTC SLOW_CLK
RWDT
RTC_WDT_CPU_RESET
RTC_WDT_SYS_RESET
RTC_WDT_CORE_RESET
RTC_WDT_INT

$$T_{hold0} = RTCCNTLWDTSTG0HOLD << (EFUSEWDTDELAYSEL + 1)$$

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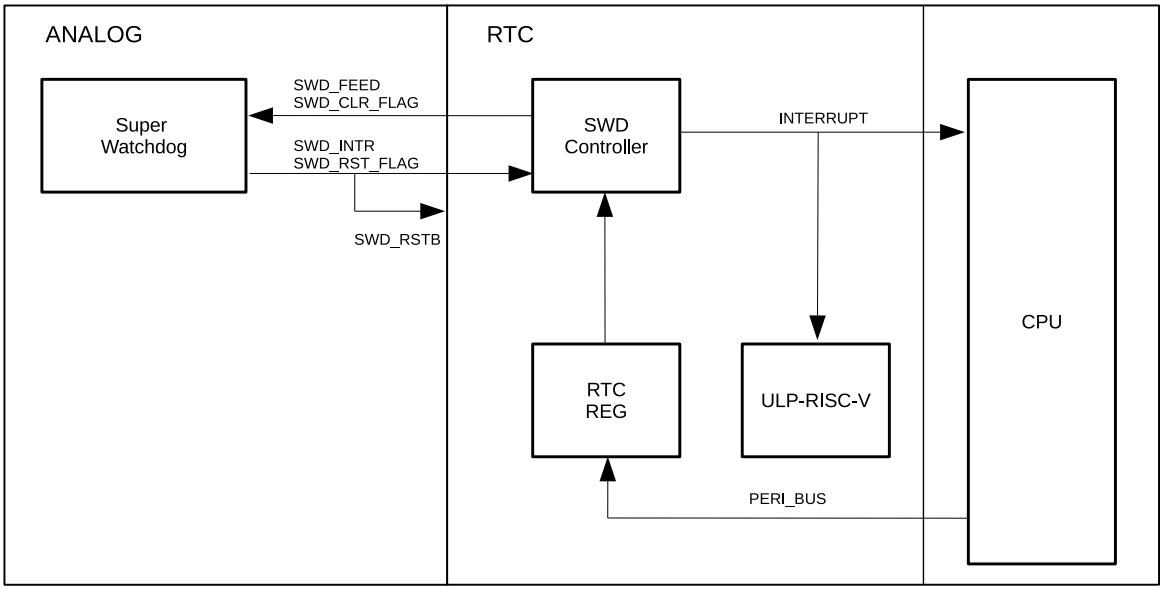
ANALOG
RTC
Super
Watchdog
SWD_FEED
SWD_CLR_FLAG
SWD_INTR
SWD_RST_FLAG
SWD_RSTB
SWD
Controller
INTERRUPT
CPU
RTC
REG
ULP-RISC-V
PERI_BUS

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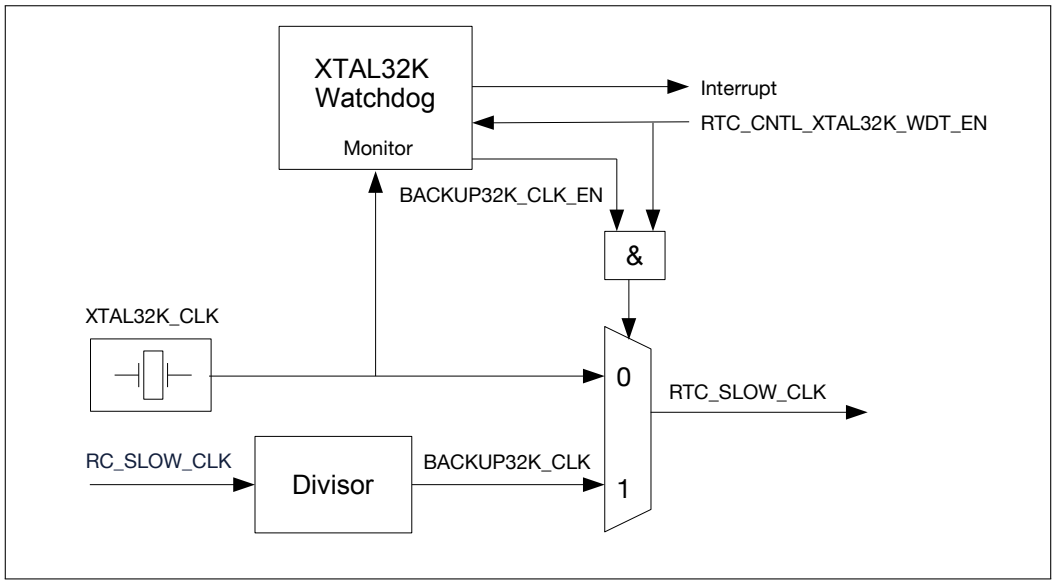
XTAL32K
Watchdog
Monitor
Interrupt
RTC_CNTL_XTAL32K_WDT_EN
BACKUP32K_CLK_EN
&
XTAL32K_CLK
0
RTC_SLOW_CLK
RC_SLOW_CLK
Divisor
BACKUP32K_CLK
1

$x_0 x_7$

$$fbackclk/4 = frcslowclk/S$$
$$S = x_0 + x_1 + ... + x_7$$

$x_0 x_7$

-
- $N = frcslowclk/fbackclk$
- $M = N/2$
- $x_n x_n$

$frcslowclk = 163000 fbackclk = 32768 S = 20 M = 2 \{x_0, x_1, x_2, x_3, x_4, x_5, x_6, x_7\} = \{2, 3, 2, 3, 2, 3, 2, 3\}$

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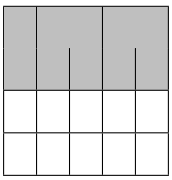

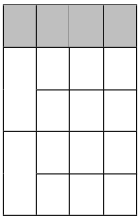

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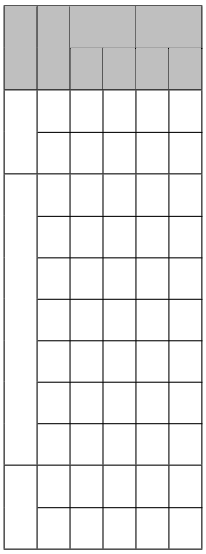

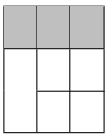

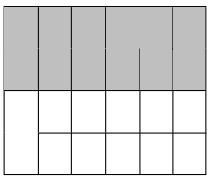

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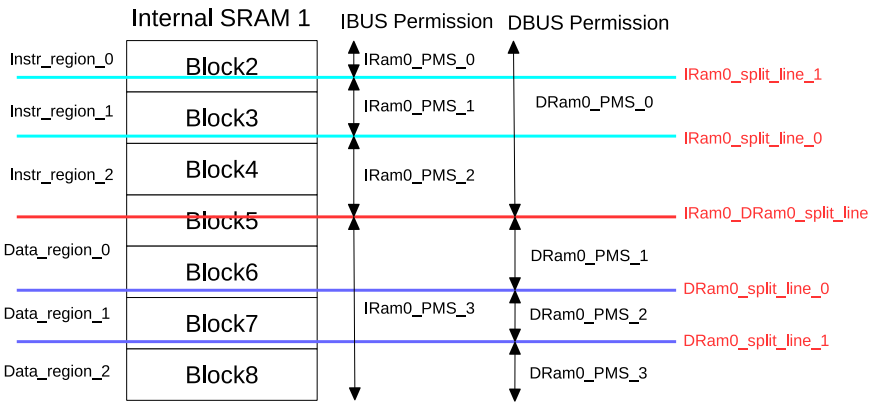
Internal SRAM 1
IBUS Permission
DBUS Permission
Instr_region_0
Instr_region_1
Instr_region_2
Data_region_0
Data_region_1
Data_region_2
Block2
Block3
Block4
Block5
Block6
Block7
Block8
IRam0_PMS_0
IRam0_PMS_1
IRam0_PMS_2
IRam0_PMS_3
DRam0_PMS_0
DRam0_PMS_1
DRam0_PMS_2
DRam0_PMS_3
IRam0_split_line_1
IRam0_split_line_0
IRam0_DRam0_split_line
DRam0_split_line_0
DRam0_split_line_1

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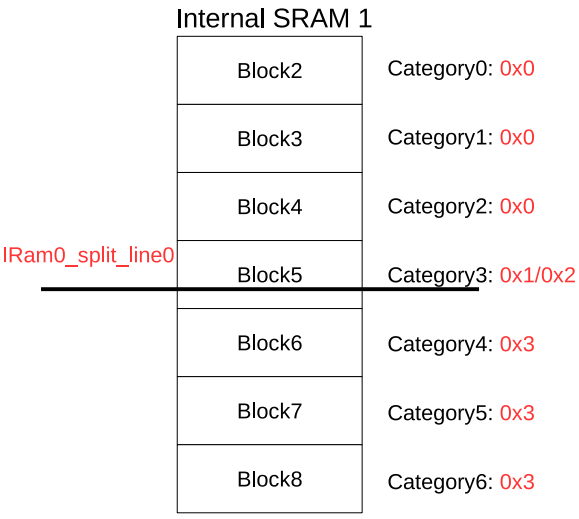
Internal SRAM 1
Block2
Block3
Block4
Block5
Block6
Block7
Block8
Category0: 0x0
Category1: 0x0
Category2: 0x0
IRam0_split_line0
Category3: 0x1/0x2
Category4: 0x3
Category5: 0x3
Category6: 0x3

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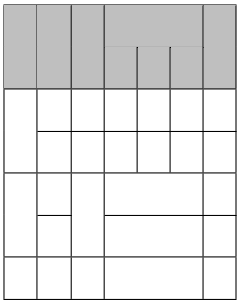

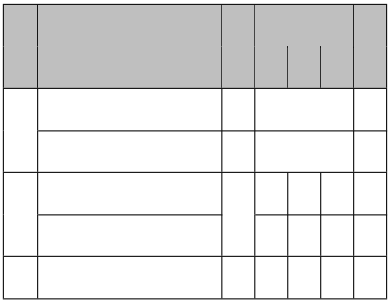

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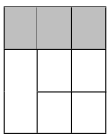

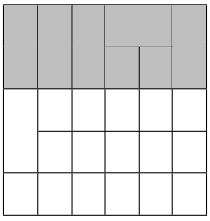

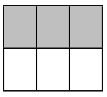

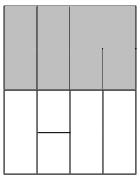

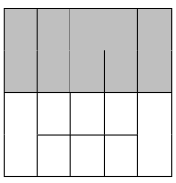

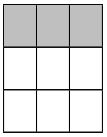

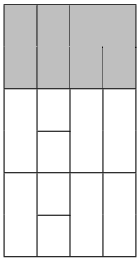

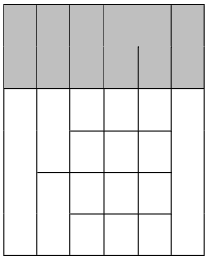

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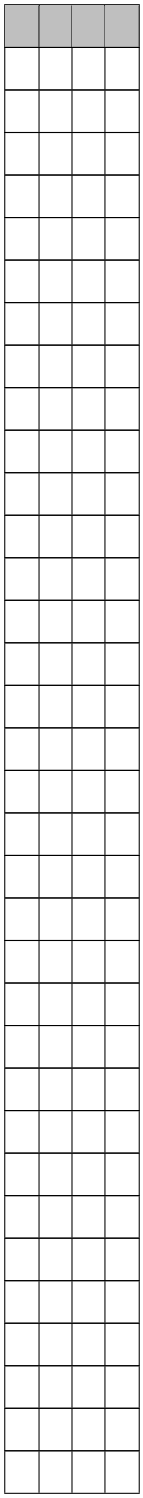

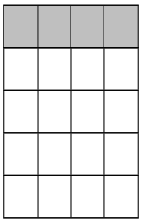

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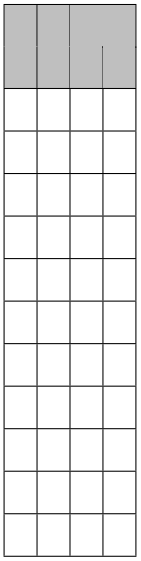

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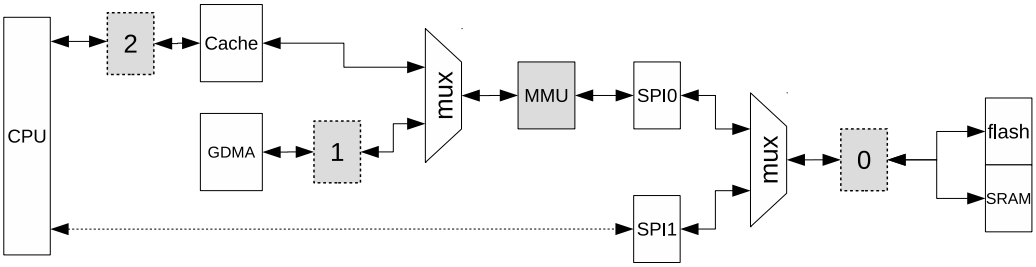
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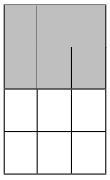

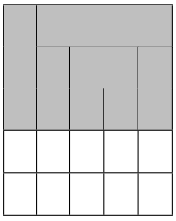

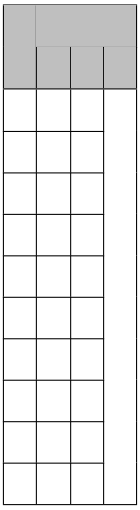

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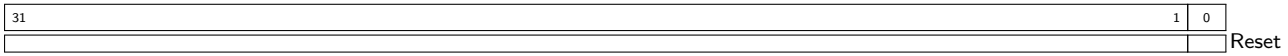
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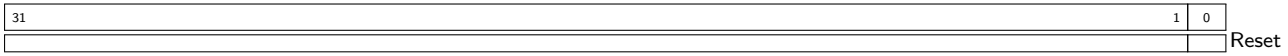
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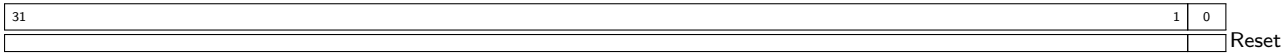
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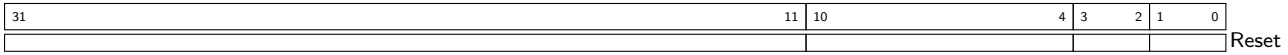
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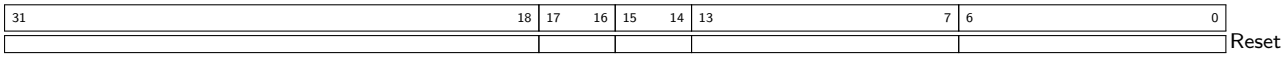
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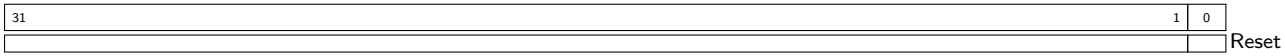
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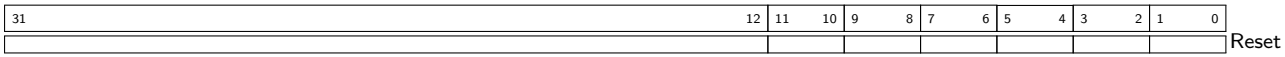
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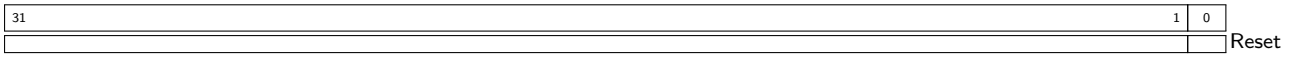
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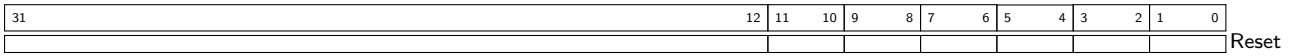
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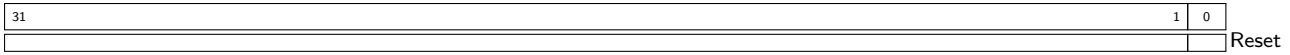
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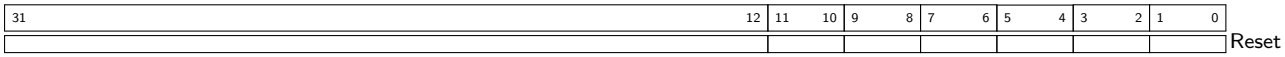
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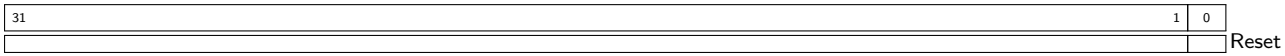
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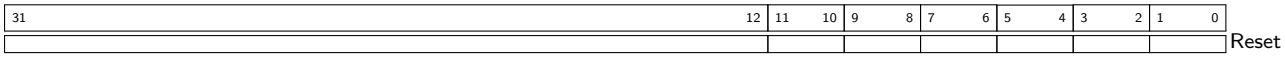
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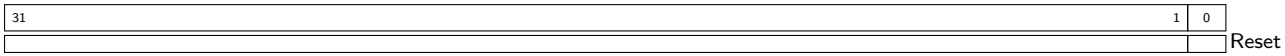
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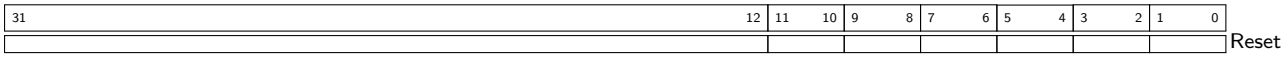
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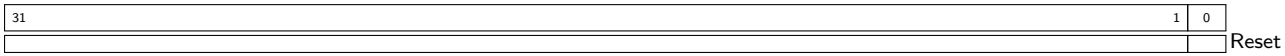
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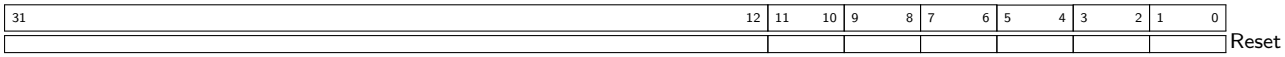
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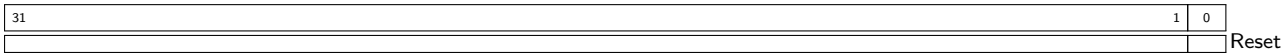
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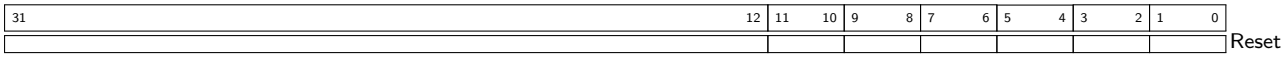
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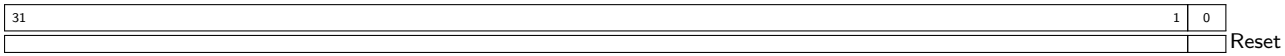
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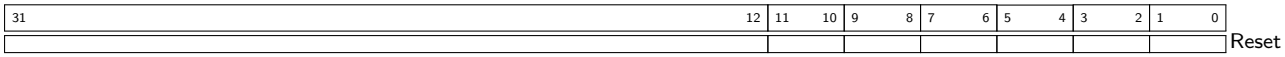
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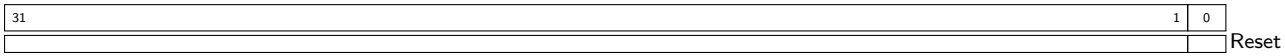
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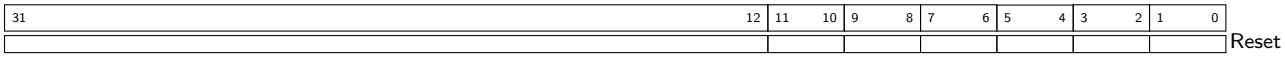
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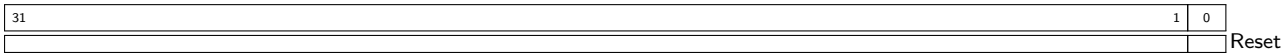
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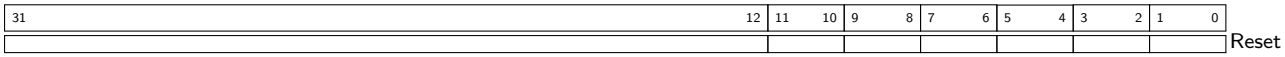
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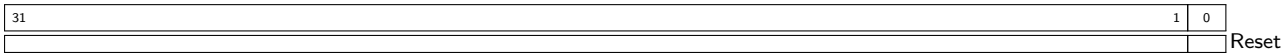
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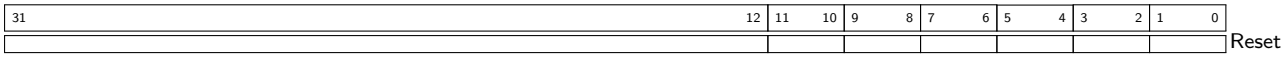
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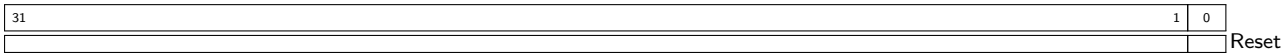
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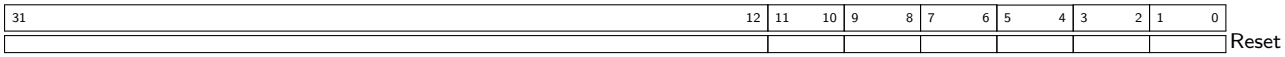
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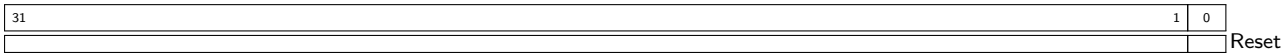
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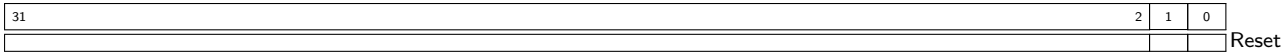
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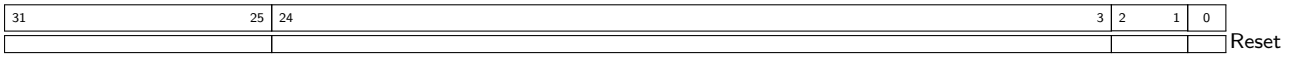
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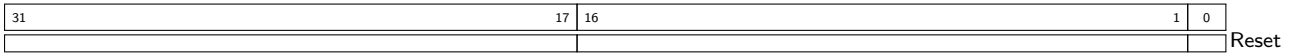
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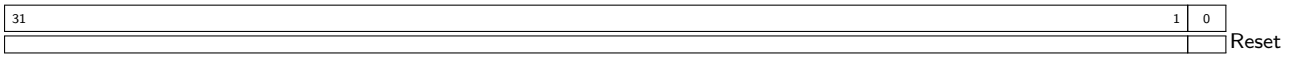
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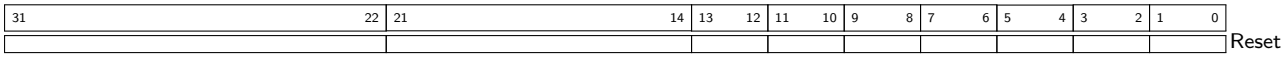
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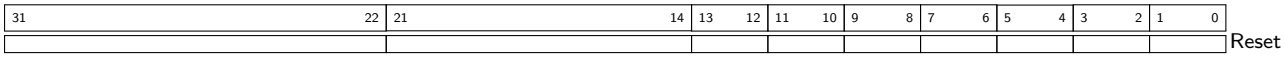
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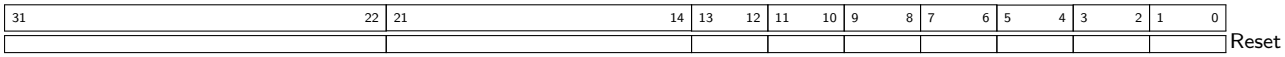
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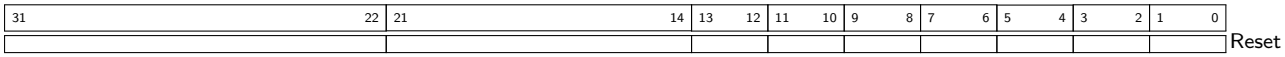
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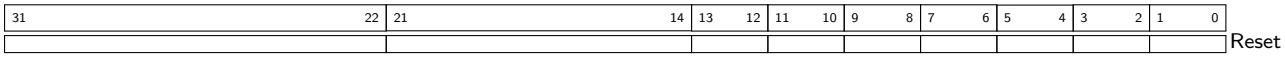
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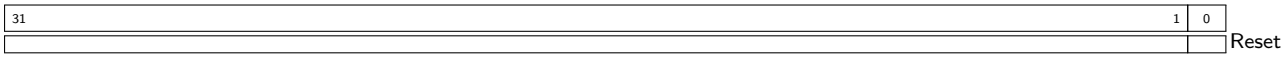
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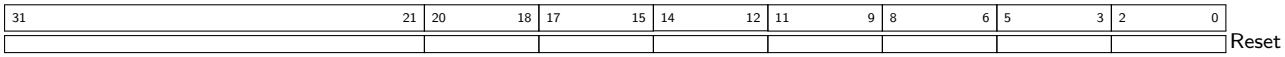
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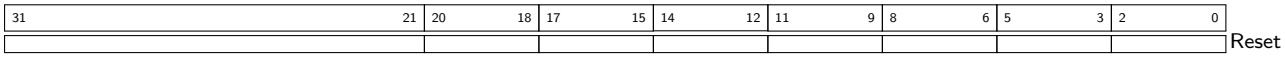
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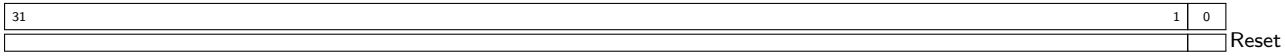
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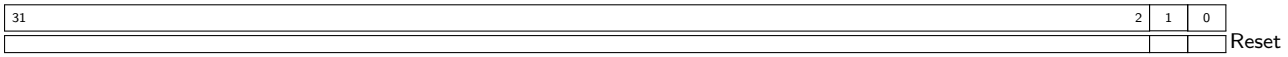
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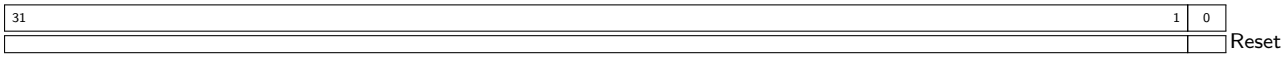
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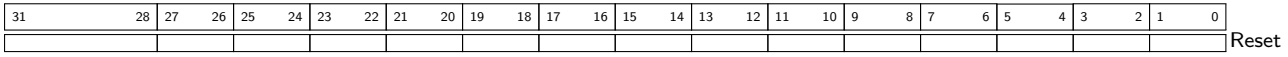
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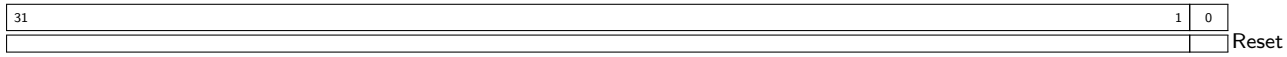
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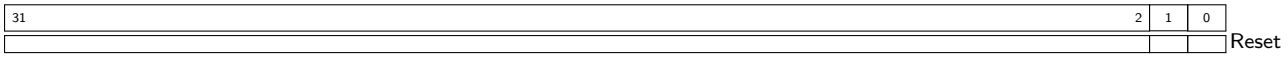
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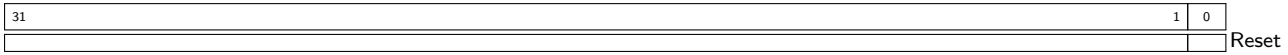
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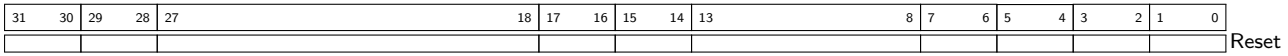
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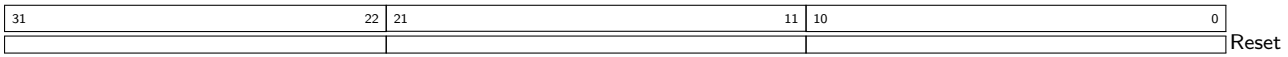
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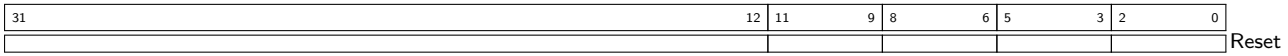
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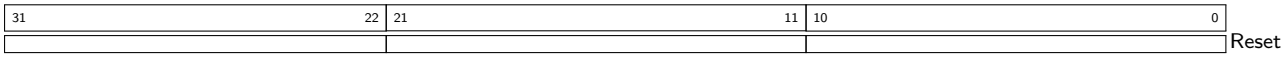
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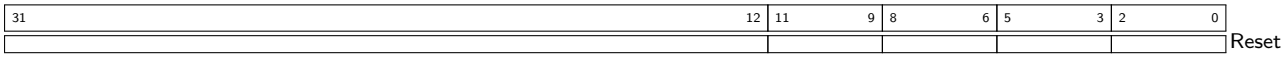
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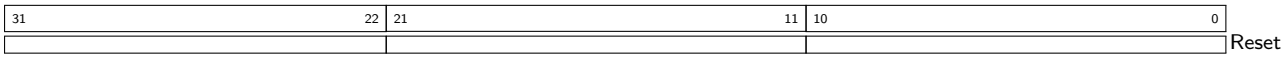
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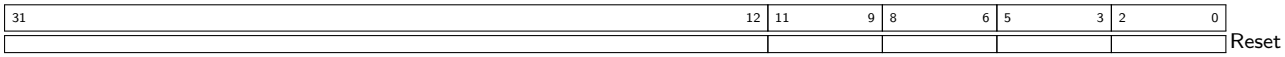
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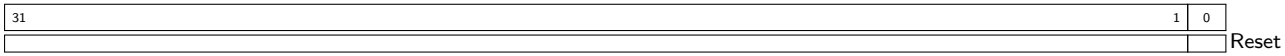
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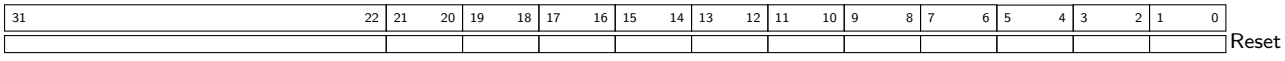
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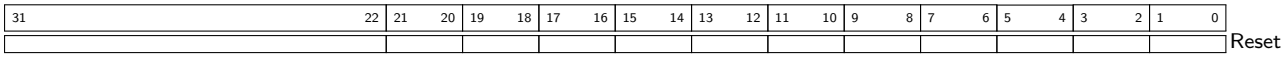
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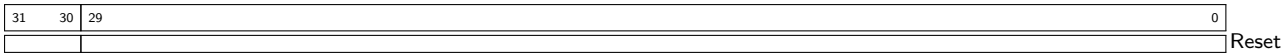
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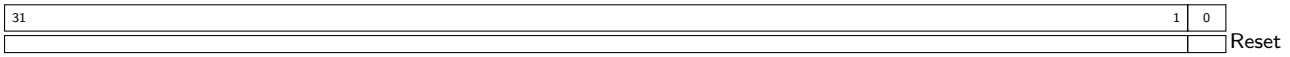
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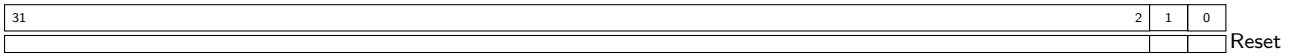
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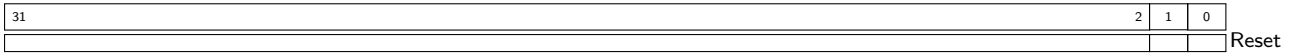
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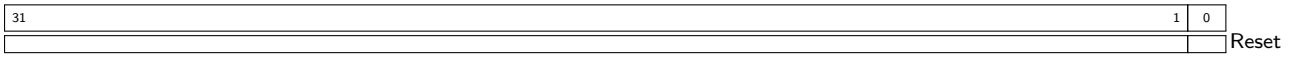
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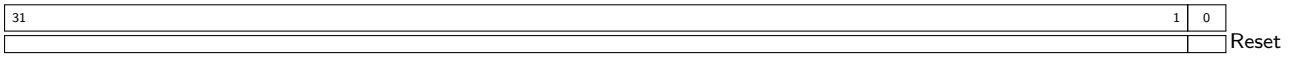
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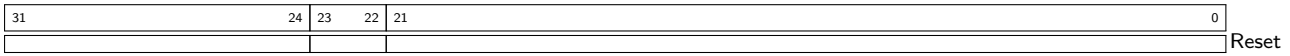
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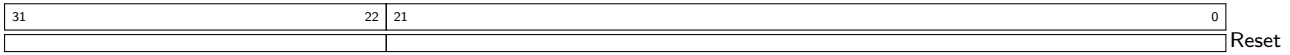
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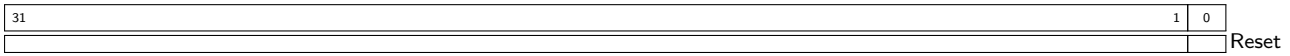
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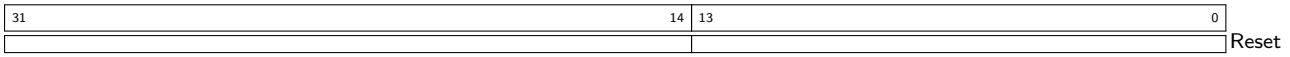
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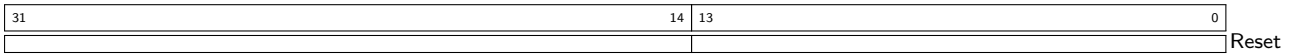
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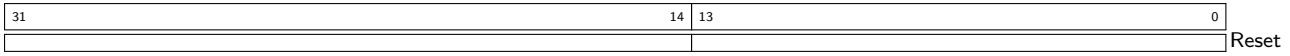
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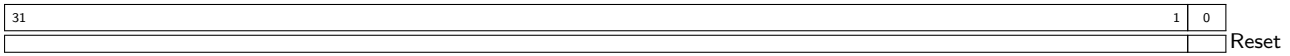
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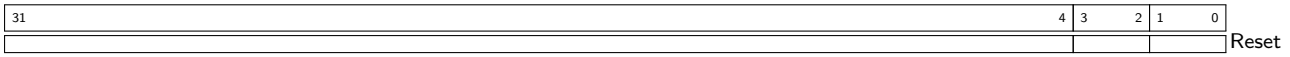
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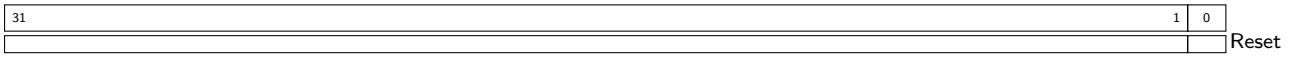
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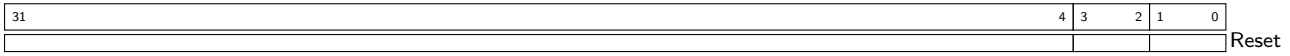
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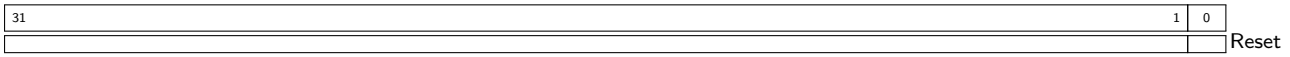
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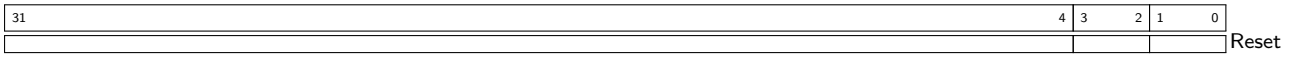
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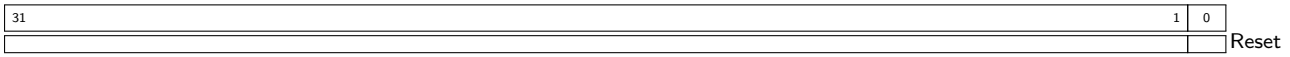
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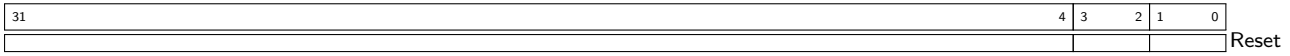
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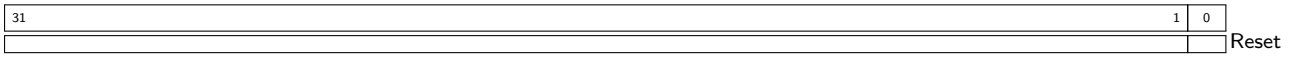
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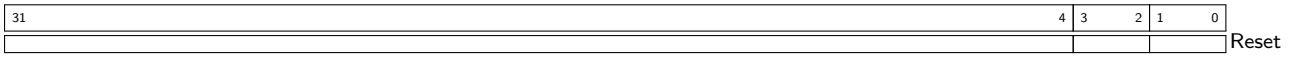
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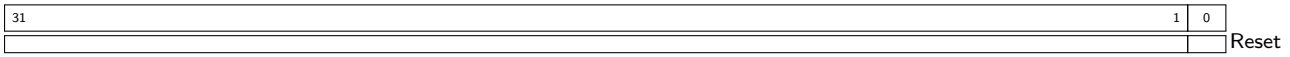
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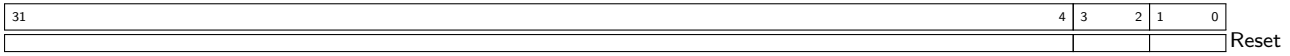
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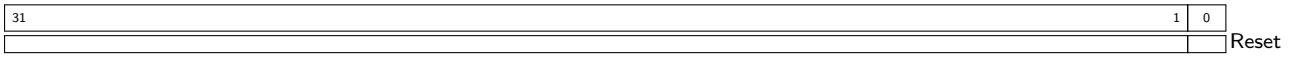
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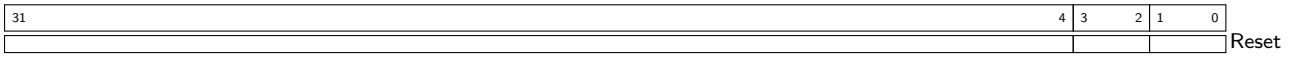
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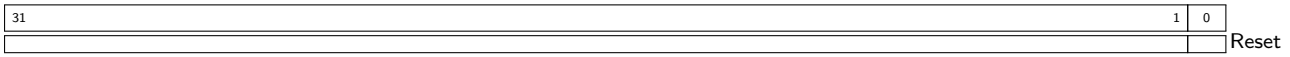
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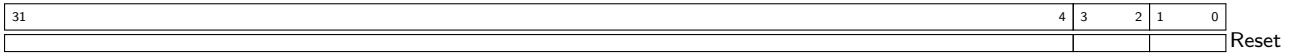
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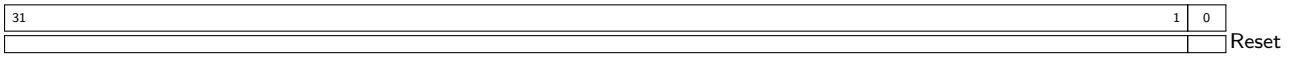
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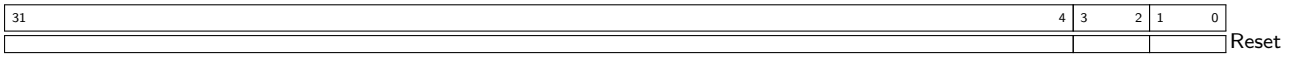
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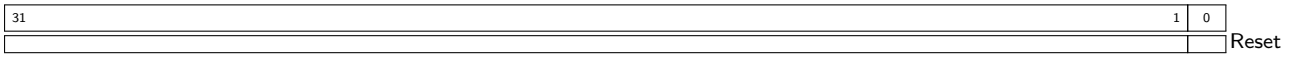
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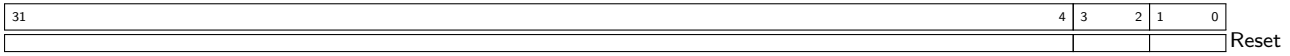
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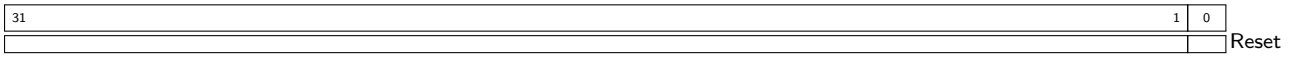
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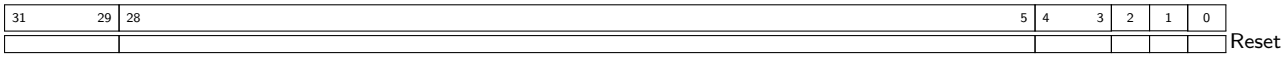
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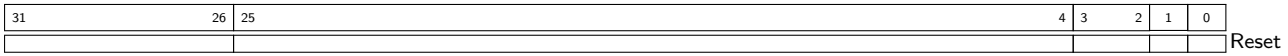
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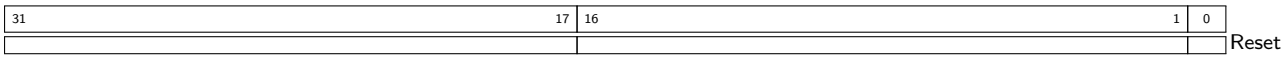
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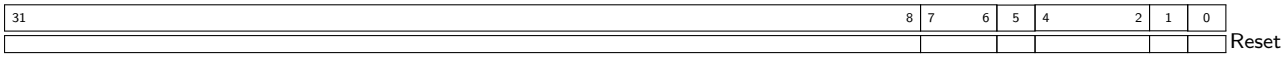
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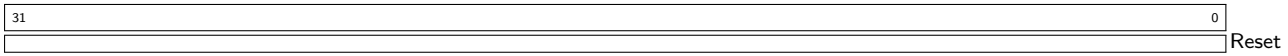
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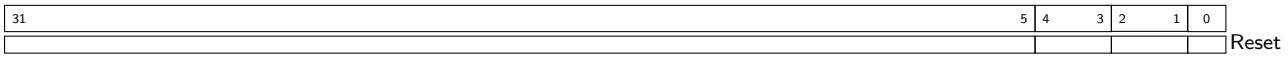
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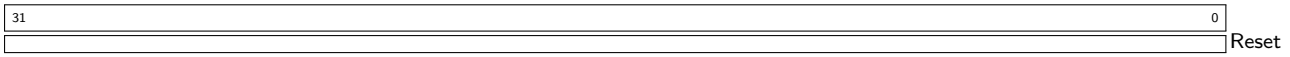
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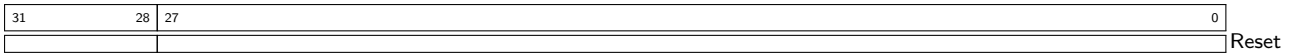
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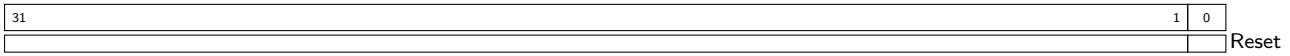
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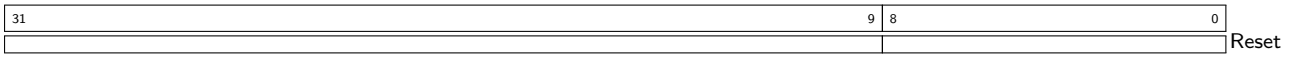
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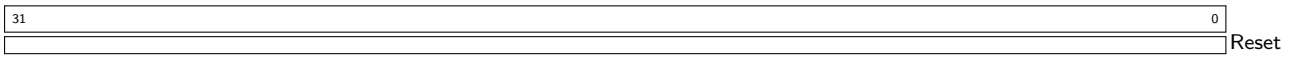
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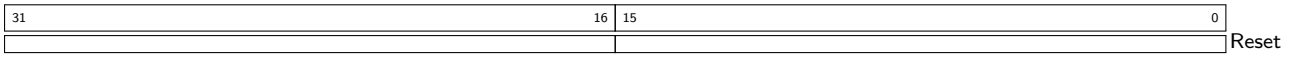
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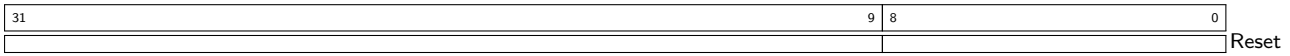
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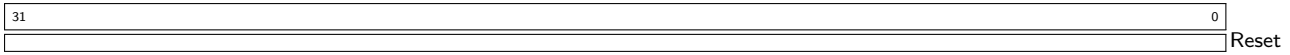
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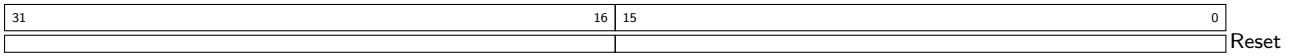
Reset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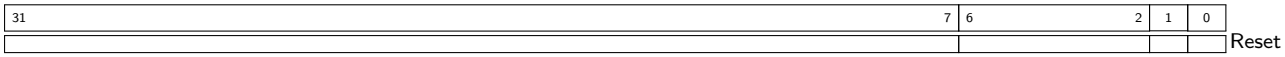
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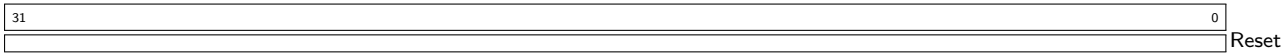
Reset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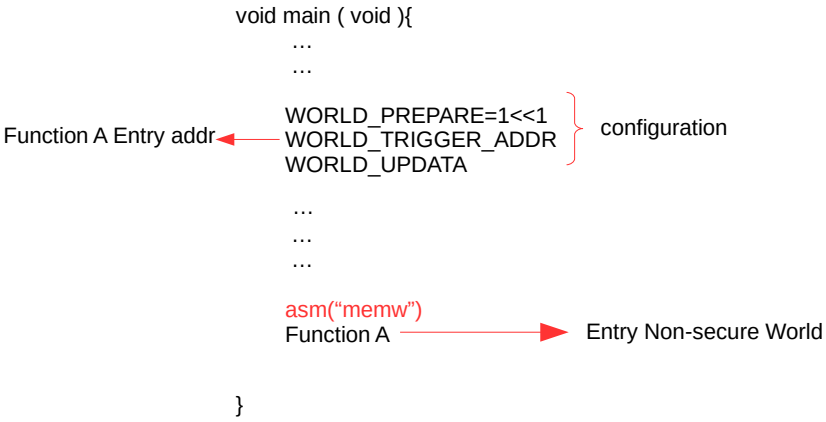
Reset


void main (void){
…
…
Function A Entry addr
WORLD_PREPARE=1<<1
WORLD_TRIGGER_ADDR
WORLD_UPDATA
configuration
…
…
…
asm(“memw”)
Function A
Entry Non-secure World
}

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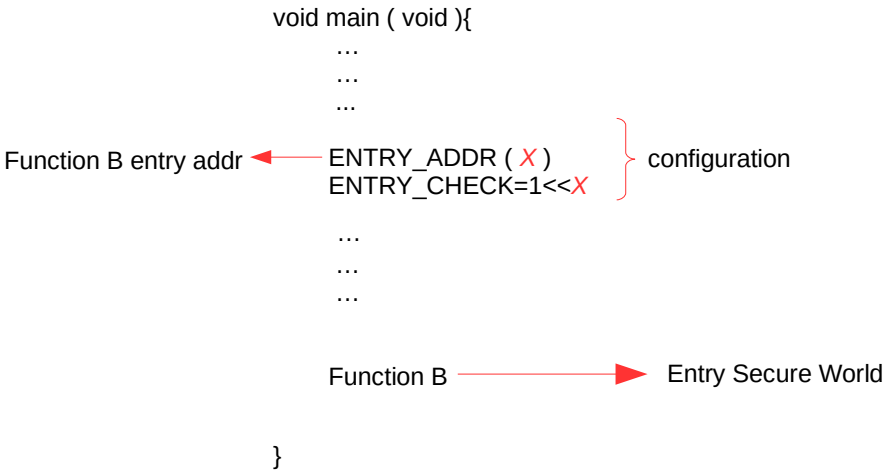
-


void main (void){
…
…
...
Function B entry addr
ENTRY_ADDR (X)
ENTRY_CHECK=1<<X
configuration
…
…
…
Function B
Entry Secure World
}

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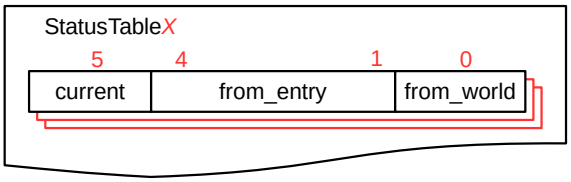
$Z \in \{3, 4, \ldots, 16$



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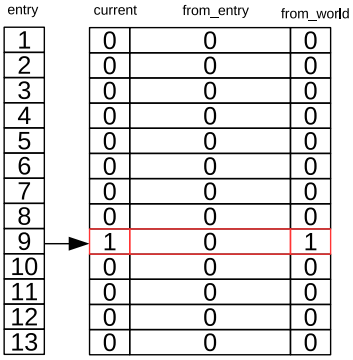
- 
entry
current
from_entry
from_world
1
2
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4
5
6
7
8
9
10
11
12
13
0 0 0
0 0 0
0 0 0
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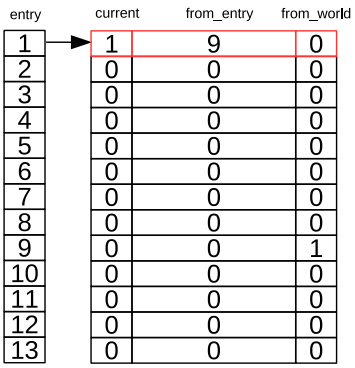
0 0 0
0 0 0
1 0 1
0 0 0
0 0 0
0 0 0
0 0 0

- 
entry
current
from_entry
from_world
1
2
3
4
5
6
7
8
9
10
11
12
13
1 9 0
0 0 0
0 0 0
0 0 0
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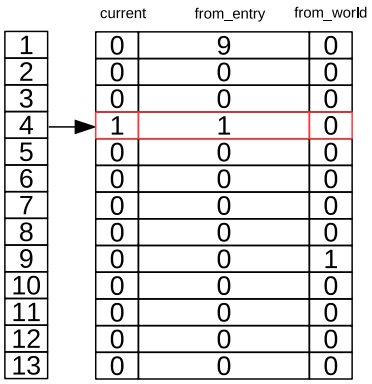
0 0 0
0 0 0
0 0 1
0 0 0
0 0 0
0 0 0
0 0 0

-

-

- 
current
from_entry
from_world
1
2
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6
7
8
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10
11
12
13
0 9 0
0 0 0
0 0 0
1 1 0
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0 0 0
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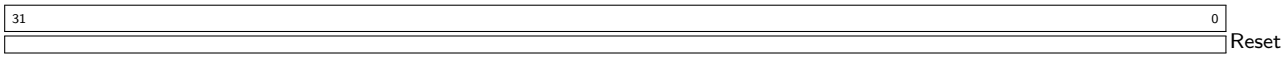
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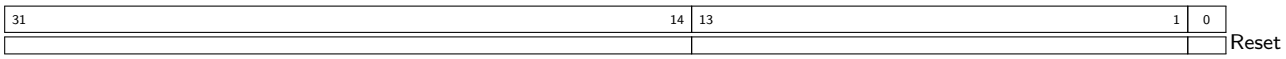
Reset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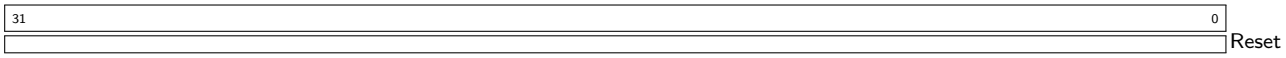
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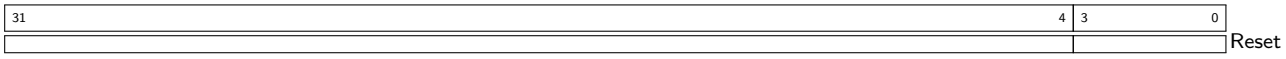
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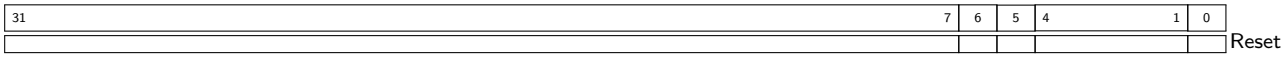
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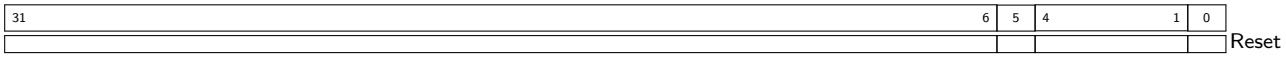
Reset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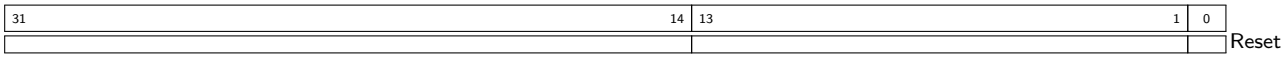
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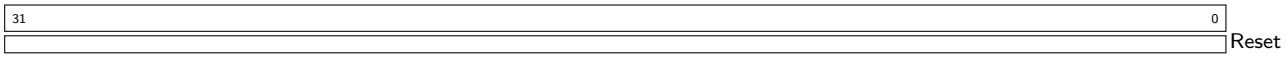
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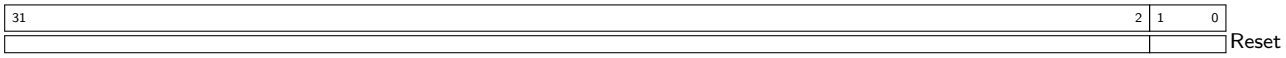
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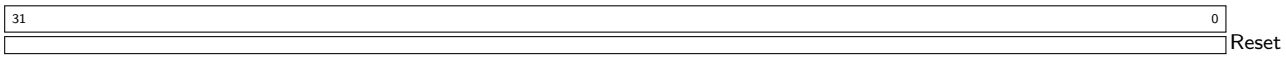
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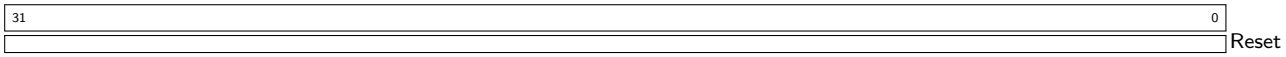
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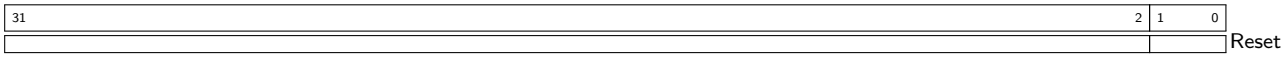
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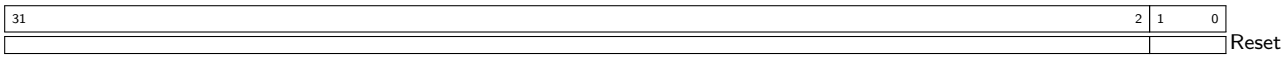
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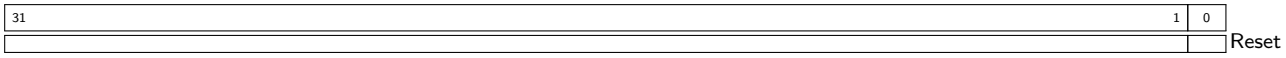
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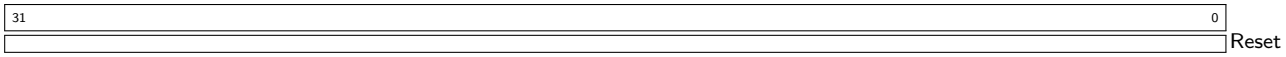
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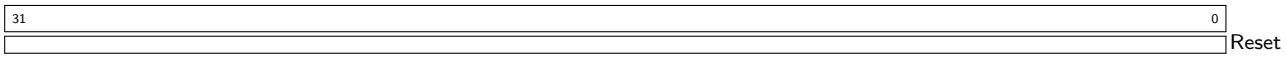
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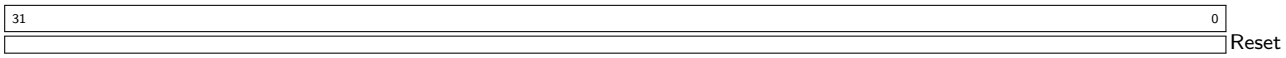
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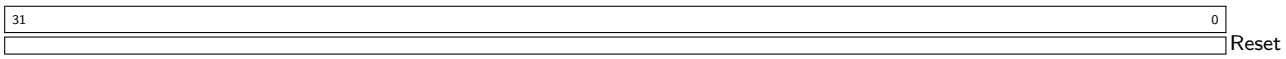
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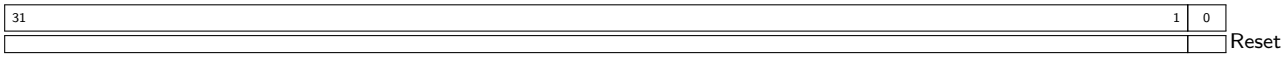
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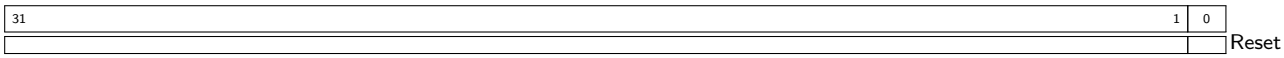
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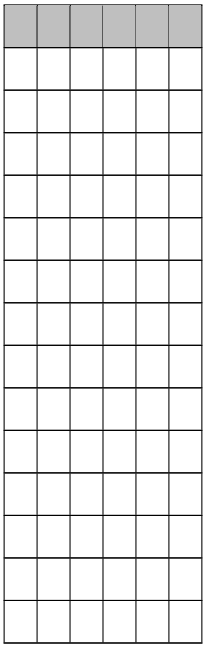

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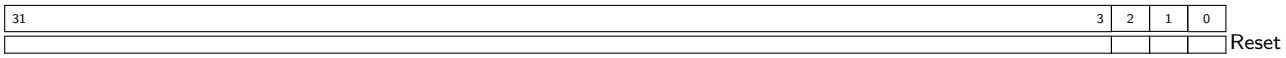
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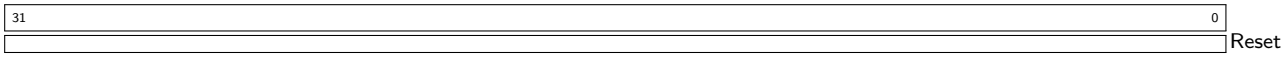
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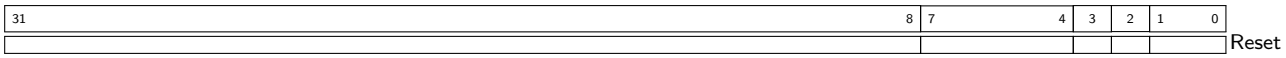
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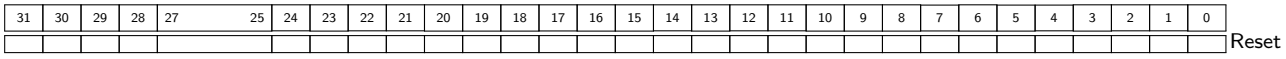
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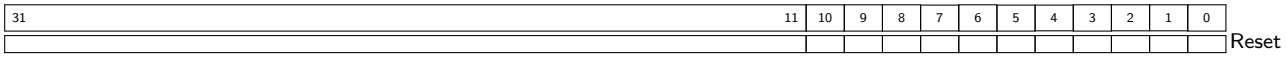
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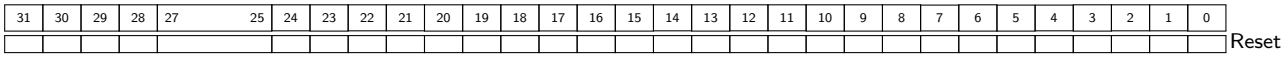
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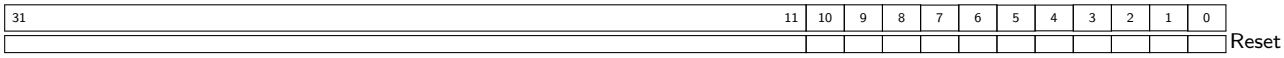
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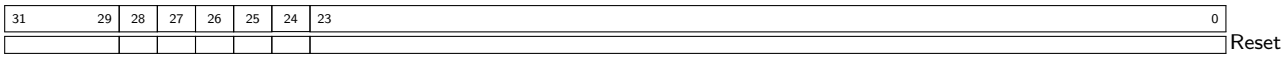
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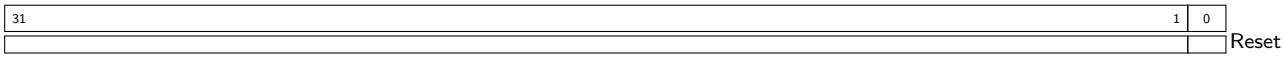
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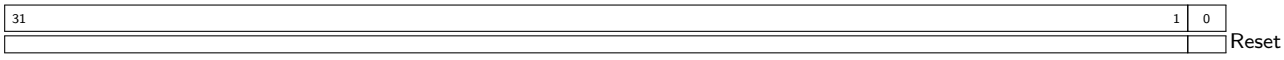
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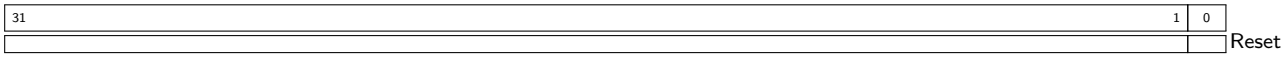
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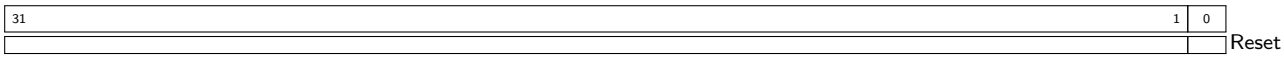
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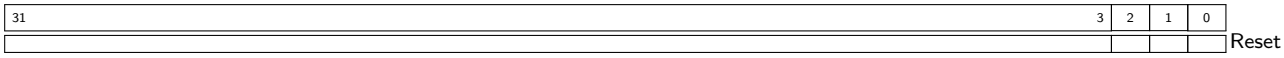
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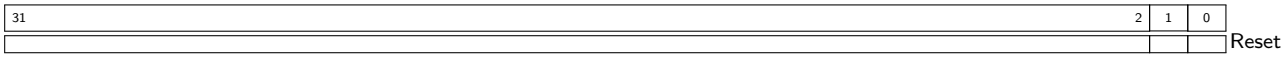
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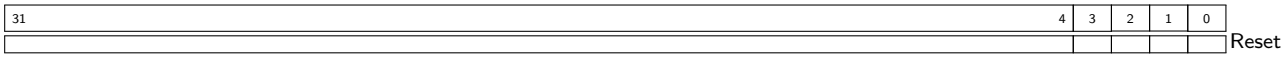
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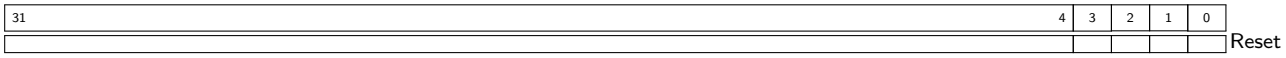
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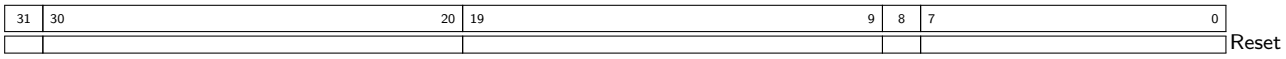
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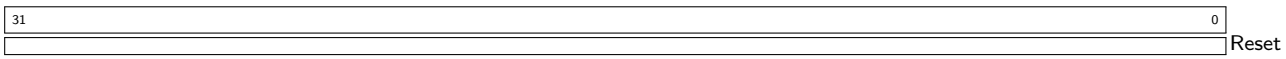
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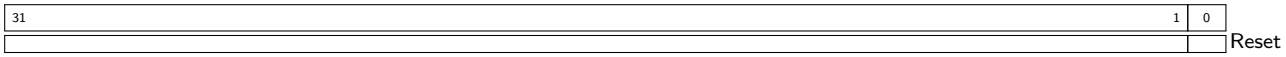
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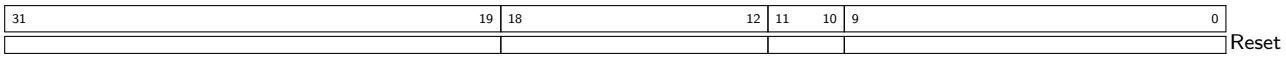
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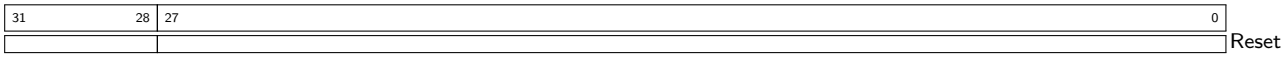
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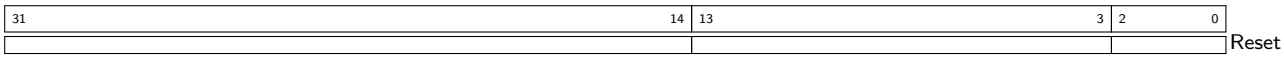
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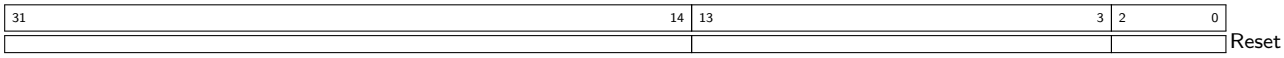
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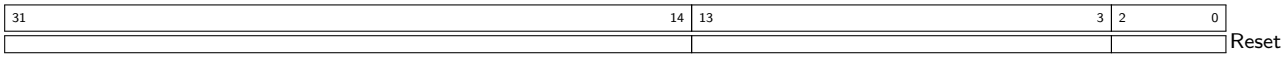
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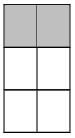

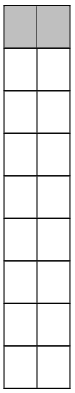

MmM

- $kkm + 1 + k \equiv 448 mod$

  m

- $kkm + 1 + k \equiv 896 mod$

m

N

- $NM^{(1)}M^{(2)}M^{(N)}i_{0\ \ 1\ \ 15}^{(i)(i)(i)}$
- $Ni_{0\ \ 1\ \ 15}^{(i)(i)(i)}$

- $_{0\ \ 1\ \ 15}^{(i)(i)(i)}$
- $_{0\ \ 15}^{(i)(i)}$

(0)

$tttttt$

t

- $1 <= t <= 9tlength = 7'h48tstring$

$8'h30 + 8'ht_0$	$1'b1$	$23'b0$

$t_0 = t$

$t_0tstring32'h38800000$

- $10 <= t <= 99tlength = 7'h50tstring$

$8'h30 + 8'ht_1$	$8'h30 + 8'ht_0$	$1'b1$	$15'b0$

$t_0 = t10t_1 = t/10$

$t_0t_1tstring32'h35368000$

- $100 <= t < 512tlength = 7'h58tstring$

$8'h30 + 8'ht_2$	$8'h30 + 8'ht_1$	$8'h30 + 8'ht_0$	$1'b1$	$7'b0$

$t_0 = t10t_1 = (t/10)10t_2 = t/100$

$t_0t_1t_2tstring32'h32333180$

M

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- - [2]
- [3]
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- [3]

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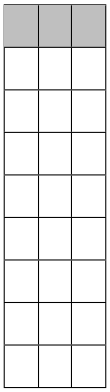

$troundup(t/32)$

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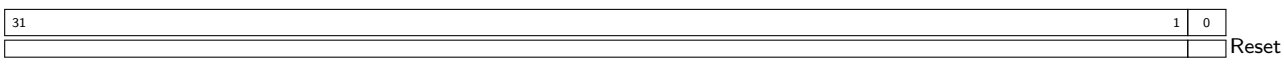
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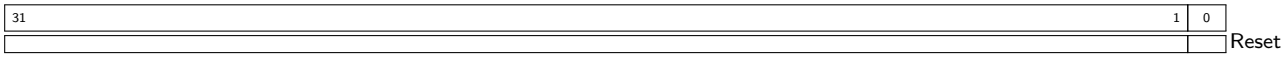
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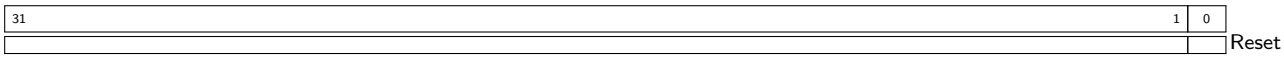
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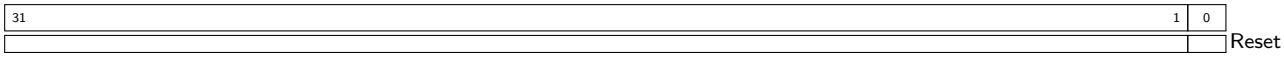
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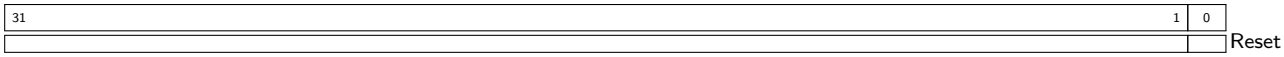
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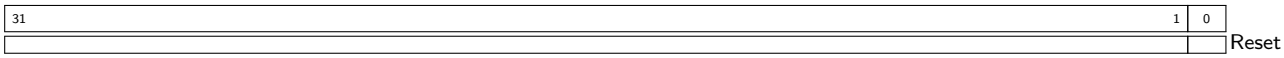
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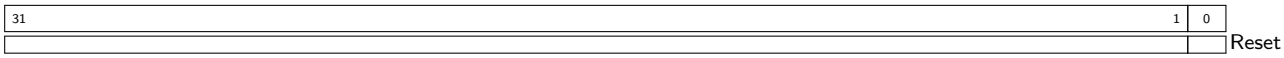
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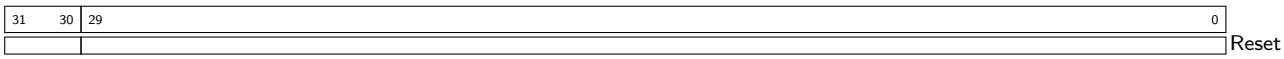
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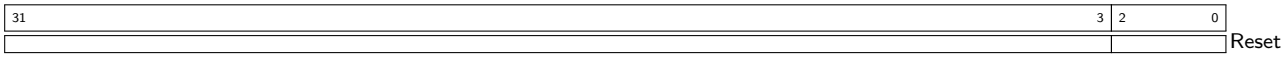
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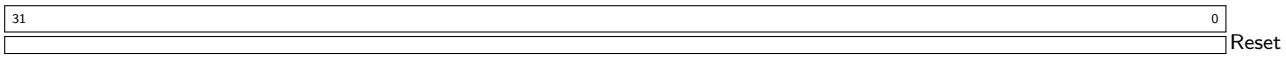
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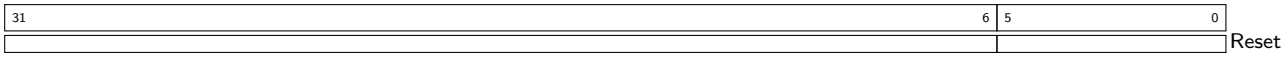
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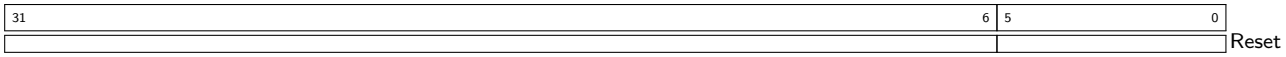
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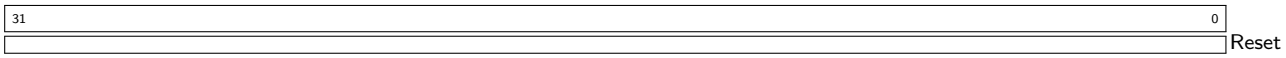
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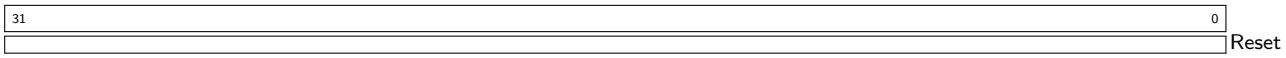
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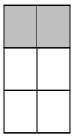

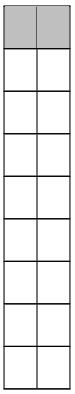

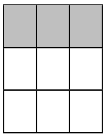

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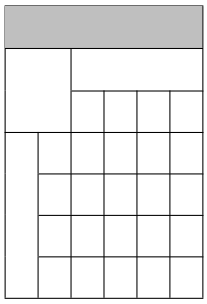

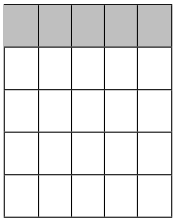

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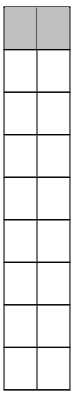

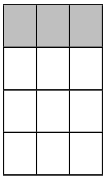

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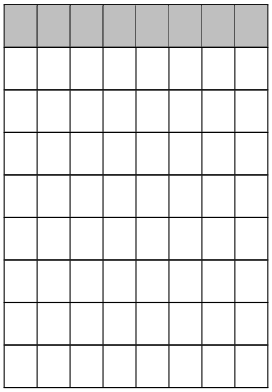
-

X YX
$X = X_1 \|\| X_2 \|\| \cdots \|\| X_{n-1} \|\| X_n$ $X_1, X_2, \cdots, X_{n-1} X_n$ $= 0$ XX $0 < <= 127 X_n^* X_n^* = X_n \|\| 0^{128-}$ $XX_1 \|\| X_2 \|\| \cdots \|\| X_{n-1} \|\| X_n^* X \|\| 0^{128-}$

-
-



3212832128

$PCPC$

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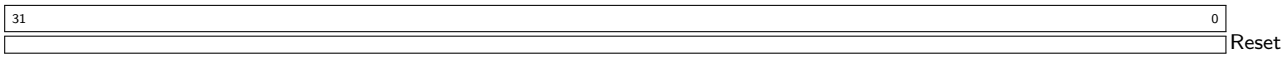
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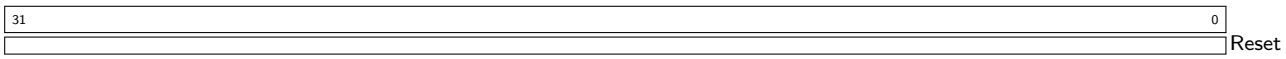
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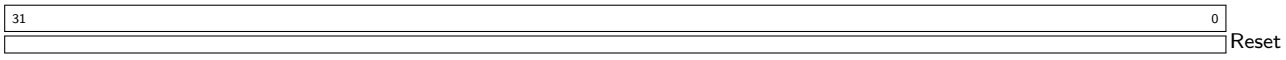
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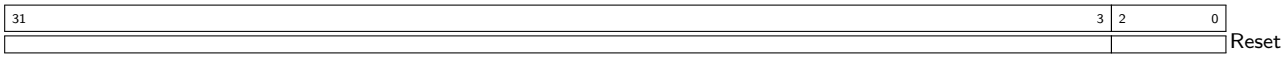
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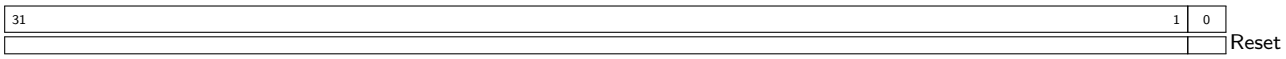
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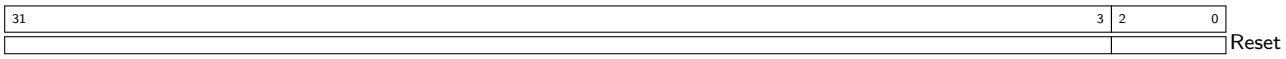
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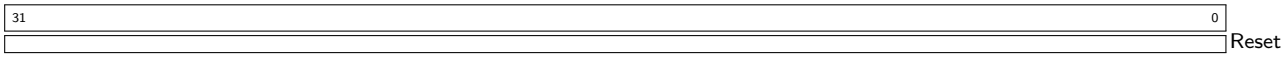
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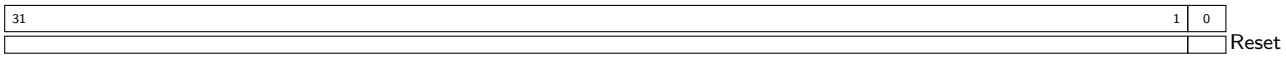
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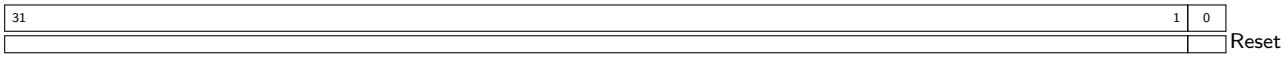
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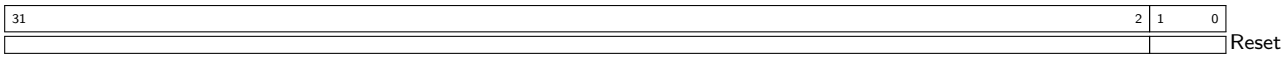
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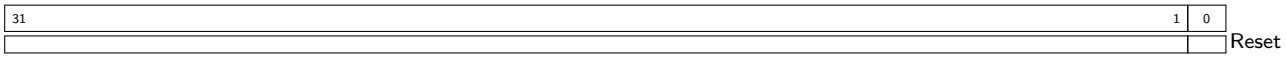
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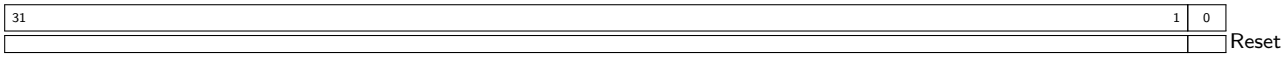
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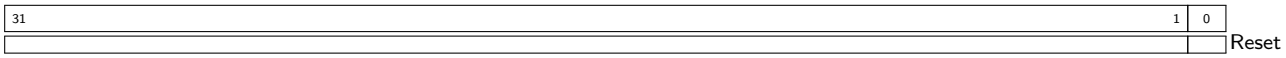
Reset


31
1
0
Reset

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$Z = X^Y \;\; MXYM\bar{r}M'$

$N = 32 \times xx \in \{1, 2, 3, \ldots, 128\} ZXYM\bar{r}NM'$

b

$$b = 2^{32}$$

b

$$n = \frac{N}{32}$$
$$Z = (Z_{n-1}Z_{n-2}\cdots Z_0)_b$$
$$X = (X_{n-1}X_{n-2}\cdots X_0)_b$$
$$Y = (Y_{n-1}Y_{n-2}\cdots Y_0)_b$$
$$M = (M_{n-1}M_{n-2}\cdots M_0)_b$$
$$\overline{r} = (\overline{r}_{n-1}\overline{r}_{n-2}\cdots \overline{r}_0)_b$$

$nZ_{n-1}\cdots Z_0X_{n-1}\cdots X_0Y_{n-1}\cdots Y_0M_{n-1}\cdots M_0\overline{r}_{n-1}\cdots \overline{r}_0b$

$Z_{n-1}X_{n-1}Y_{n-1}M_{n-1}\overline{r}_{n-1}ZXYMZ_0X_0Y_0M_0\overline{r}_0$

$R = b^n\overline{r} = R^2 \ \ M$

$$M^{-1} \times M + 1 = R \times R^{-1}$$
$$M' = M^{-1} \ \ b$$

$(\frac{N}{32} - 1)$

M'

$X_iY_iM_i\overline{r}_ii \in \{0, 1, \ldots, n-1\}b$

$Z_ii \in \{0, 1, \ldots, n-1\}$

$X_i\overline{r}_i$

$Z = X \times Y \ \ M\overline{r}M'$

$(\frac{N}{32} - 1)$

M'

$X_i Y_i M_i \overline{r}_i i \in \{0, 1, \ldots, n-1\} b$

$Z_i i \in \{0, 1, \ldots, n-1\}$

$X_i Y_i M_i M' \overline{r}_i$

$Z = X \times YZXYN = 32 \times xx \in \{1, 2, 3, \ldots, 64\} \hat{N} Z2 \times N$

$(\frac{\hat{N}}{32} - 1)(\frac{N}{16} - 1)$

$X_i Y_i \in \{0, 1, \ldots, n-1\} b n \frac{N}{32}$

$X_i i \in \{0, 1, \ldots, n-1\} i Y_i i \in \{0, 1, \ldots, n-1\} in + i4 \times (n + i)$

$Z_i i \in \{0, 1, \ldots, \hat{n} - 1\} \hat{n} 2 \times n$

$X_i Y_i$

$Z = X^Y \ \ MY$

Y

$$Y = \widetilde{(Y_{N-1}} \widetilde{Y_{N-2}} \cdots \widetilde{Y_{t+1}} \widetilde{Y_t} \widetilde{Y_{t-1}} \cdots \widetilde{Y_0})_2$$

- NY

- $\widetilde{Y_t}$
- $\widetilde{Y_{N-1}}\widetilde{Y_{N-2}}\widetilde{Y_{t+1}}$
- $\widetilde{Y_{t-1}}\widetilde{Y_{t-2}}\widetilde{Y_0}mtm\widetilde{Y_{t-1}}\widetilde{Y_{t-2}}, \cdots, \widetilde{Y_0}t - m$

- $\widetilde{Y_i i} > \alpha\alpha\alpha N\alpha t\widetilde{Y_{N-1}}\widetilde{Y_{N-2}}\widetilde{Y_{t+1}}\alpha tZ = X^Y \ \ M$
- Y

$Z = X^Y \ \ MNY\alpha$

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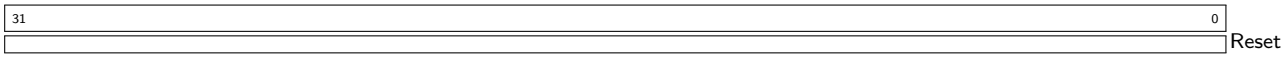
-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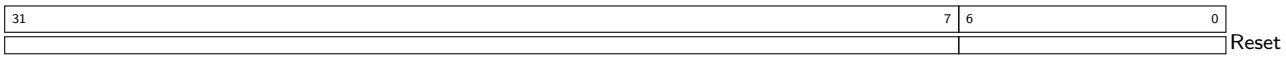
31
7
6
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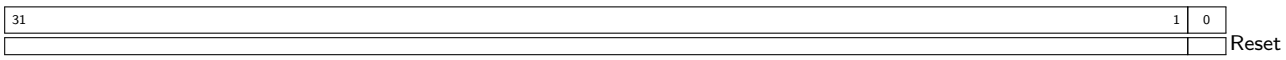
Reset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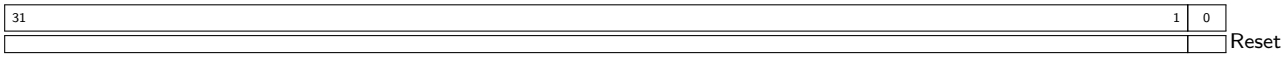
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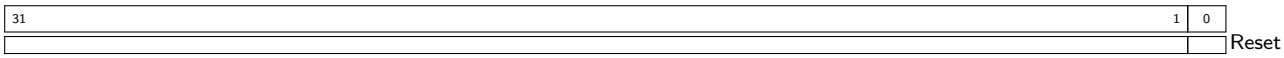
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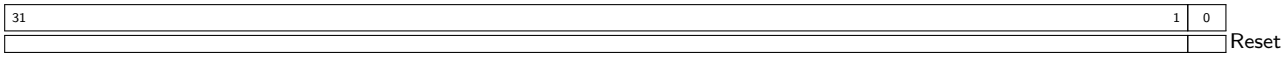
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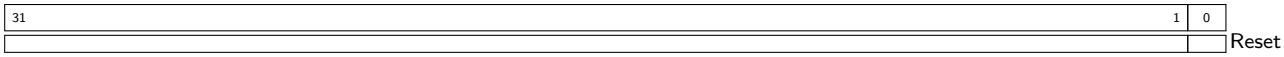
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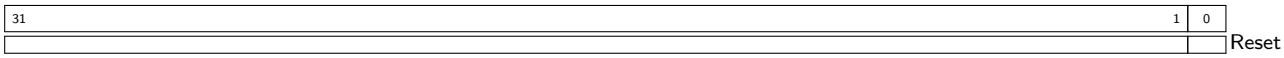
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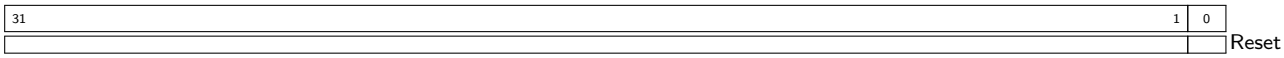
31
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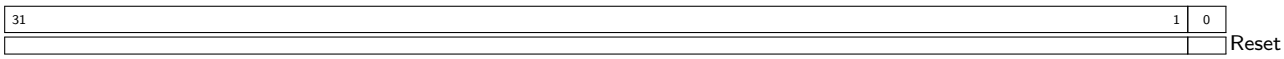
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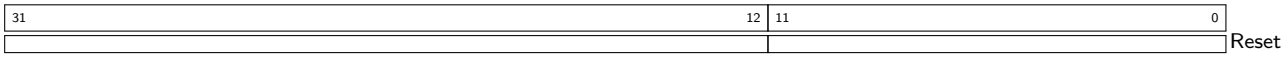
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12
11
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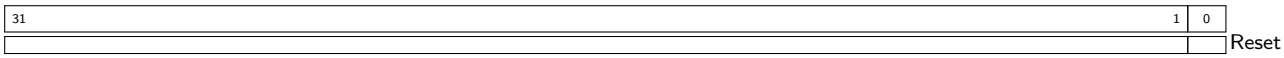
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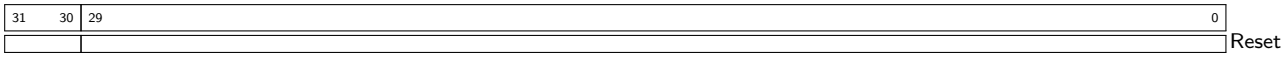
Reset


31
30
29
0
Reset

-
-
-
-
-

-
-
-
-
-

$yy(y-4)(y-4)$

m

$n >= 1$

- $n = n + 1$

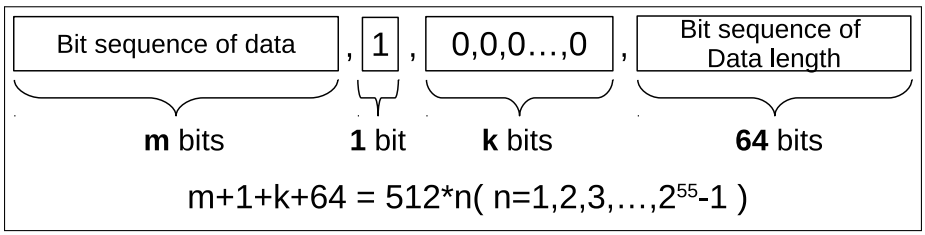
- $n = 1$

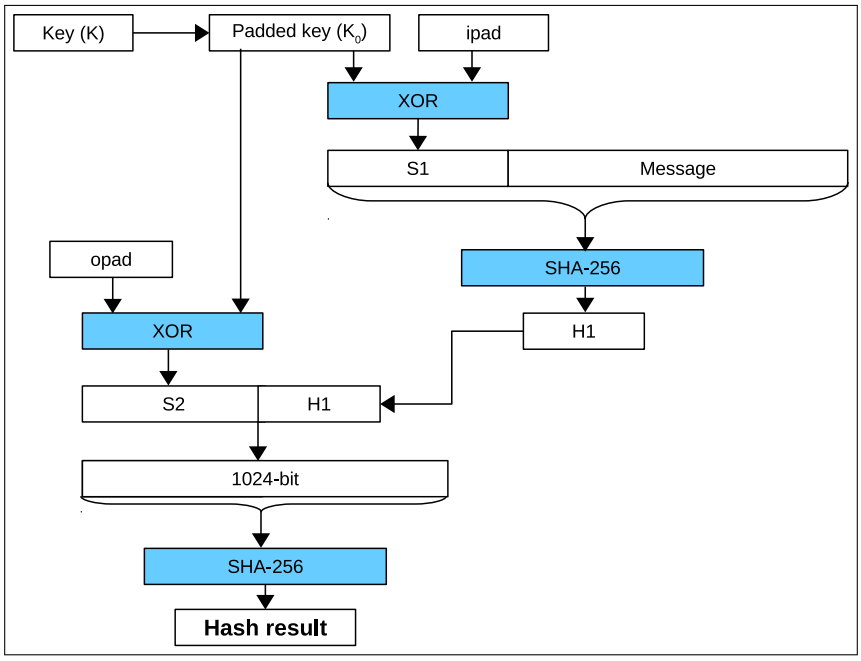
  $n = n + 1$

m

$km + 1 + k \equiv 448 (mod 512)$

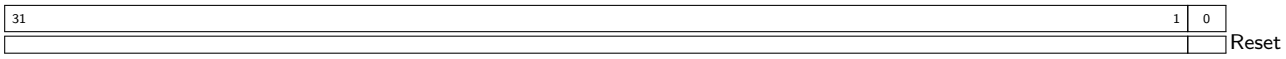
m

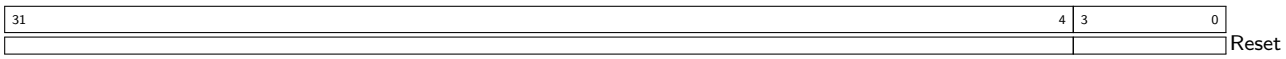

Bit sequence of data
1
0,0,0…,0
Bit sequence of Data length
m bits
1 bit
k bits
64 bits
m+1+k+64 = 512*n(n=1,2,3,…,2^55-1)

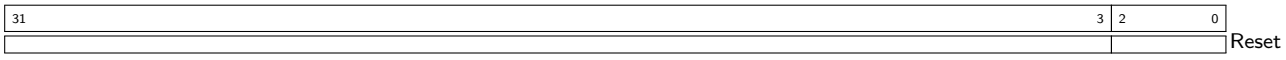

Key (K)
Padded key (K0)
ipad
XOR
S1
Message
opad
SHA-256
XOR
H1
S2
H1
1024-bit
SHA-256
Hash result

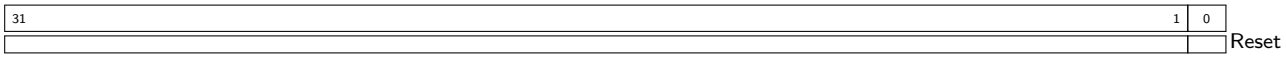
00

0


31
1
0
Reset


31
4
3
0
Reset


31
3
2
0
Reset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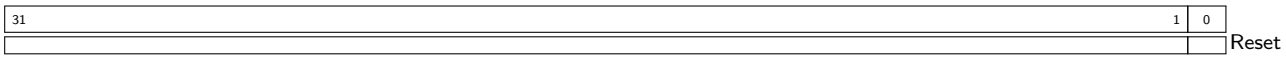
Reset


31
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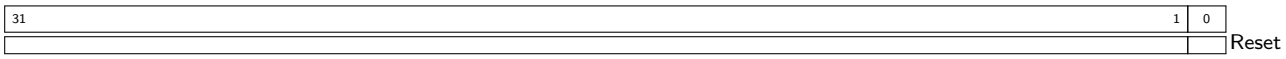
Reset


31
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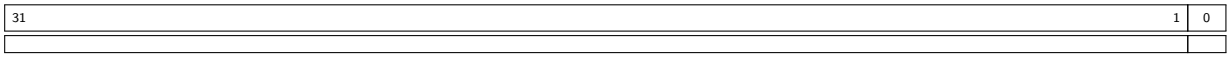
0
Reset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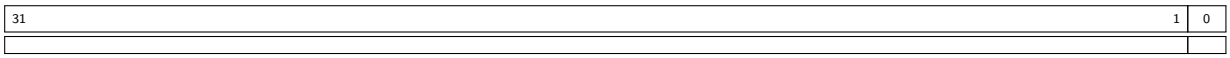
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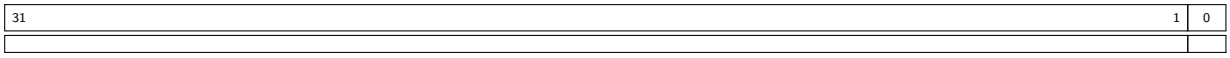
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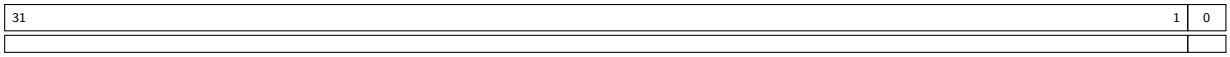
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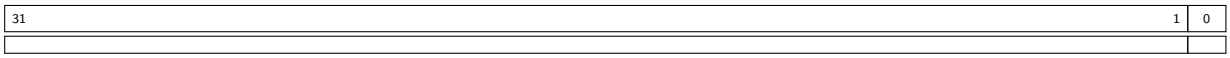
Reset


31
1
0
Reset

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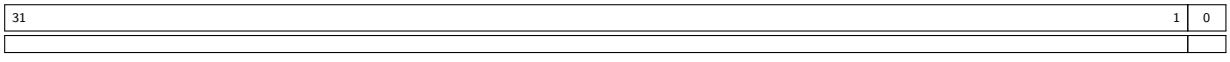
31
1
0
Reset

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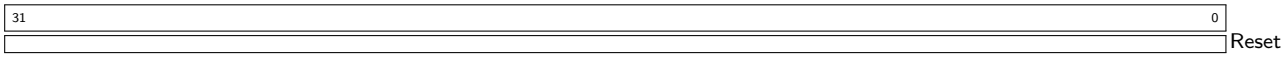
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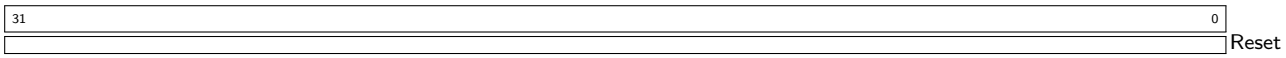
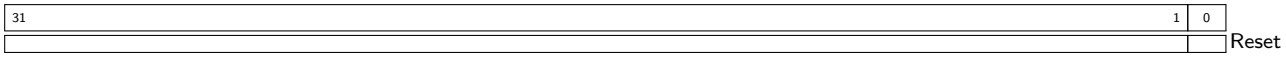
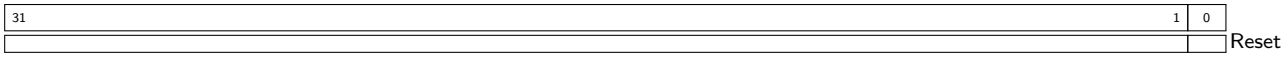
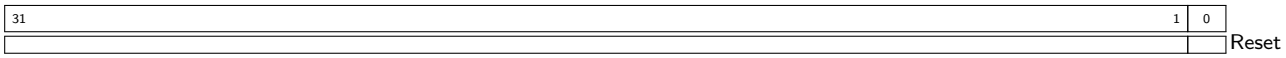
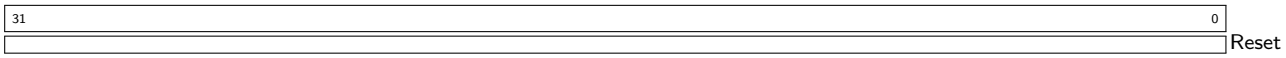
0
Reset

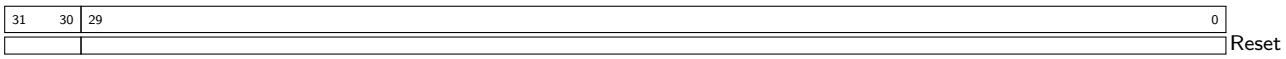

31
0
Reset


31
1
0
Reset


31
1
0
Reset


31
1
0
Reset


31
0
Reset


31
30
29
0
Reset

-
-
-

$Z = X^Y \quad MZXYM$

$DSKEYHMACKEY$

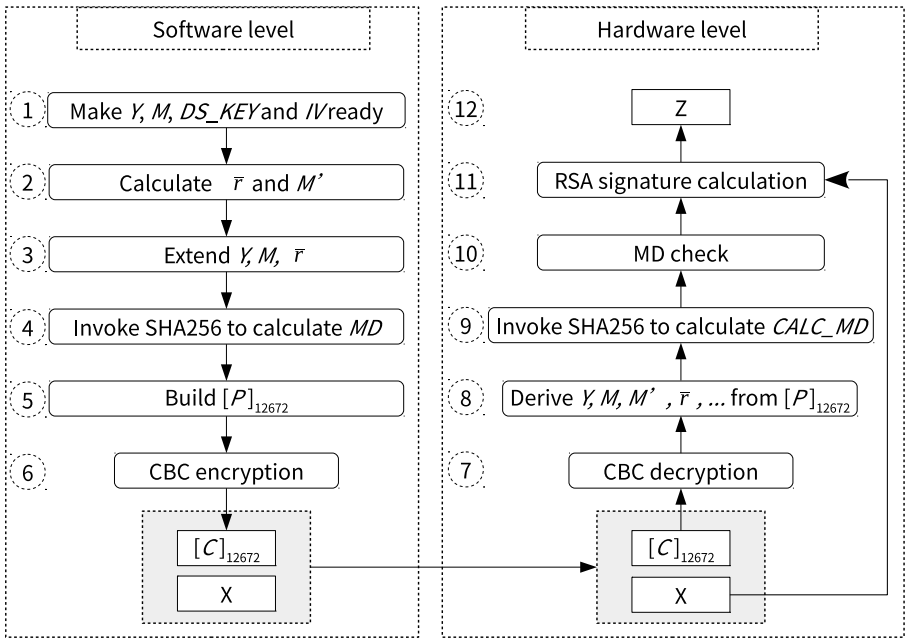
XZ

- $^s \qquad s$
- $[x]_s \qquad ssxx^s x[Y]_{40968}[x]_t(s-t)s[x]_{s8} = 00000101_{16} = 0000010100000000_{16} = 0000000000000101_{8} = 00010011_{16} = 0001001100000000_{16} = 0000000000010011$
- $||$

$YM\bar{r}M'YM$

$YM\bar{r}M'CCC$

$Z = X^Y \quad MN = 32 \times xx \in \{1, 2, 3, \ldots, 128\}ZXYM\bar{r}NM'$



C

- $YM[L]_{32} = \frac{N}{32} - 1[L]_{32}32[HMACKEY]_{256}[DSKEY]_{256}DSKEY[HMACKEY]_{256}1^{256}[IV]_{128}$
- $\overline{r}M'M$
- $YM\overline{r}[Y]_{4096}[M]_{4096}[\overline{r}]_{4096}YM\overline{r}$
- $[MD]_{256}[Y]_{4096}||[M]_{4096}||[\overline{r}]_{4096}||[M']_{32}||[L]_{32}||[IV]_{128}$
- $[P]_{12672}[Y]_{4096}||[M]_{4096}||[\overline{r}]_{4096}||[MD]_{256}||[M']_{32}||[L]_{32}||[\beta]_{64})[\beta]_{64}[]_{64}[\beta]_{64}P$
- $C[C]_{12672}[P]_{12672}[DSKEY]_{256}[IV]_{128}C$

$CXIV$

$CPCDSKEYIVIV[IV]_{128}[DSKEY]_{256}HMACKEY[DSKEY]_{256}[HMACKEY]_{256}$

$[Y]_{4096}[M]_{4096}[\overline{r}]_{4096}[M']_{32}[L]_{32}[\beta]_{64}$

- $[CALCMD]_{256}[Y]_{4096}||[M]_{4096}||[\overline{r}]_{4096}||[M']_{32}||[L]_{32}||[IV]_{128}[CALCMD]_{256}[MD]_{256}$
- $[\beta]_{64}[\beta]_{64}$

$XYM\overline{r}M'X^Y \;\; MLZZ = X^Y \;\; M$

$CXIV$

$DSKEYHMACKEY$

$CXIV$

$DSKEY$

-
- $DSKEY$

$IVIV$

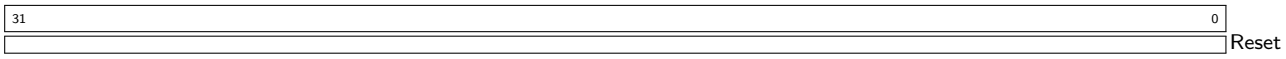
$XX_i i \in \{0, 1, \ldots, n-1\} n = \frac{N}{32} bXN$

$CC_i i \in \{0, 1, \ldots, 395\} b$

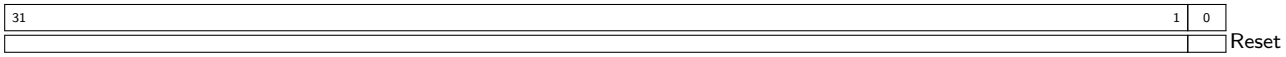
- Z
- Z
- Z
- Z

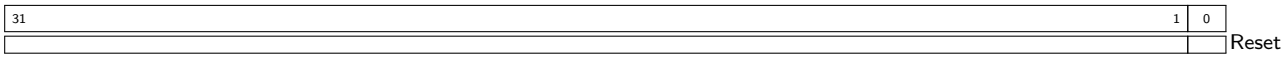
$Z_i i \in \{0, 1, \ldots, n-1\} n = \frac{N}{32} Z$

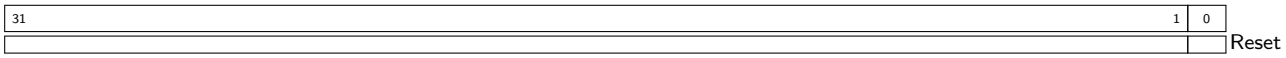
	IV		
	IV		
	IV		
	IV		
	$DSKEY$		

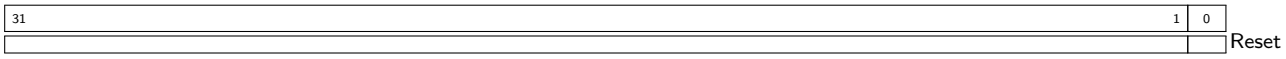

31
0
Reset

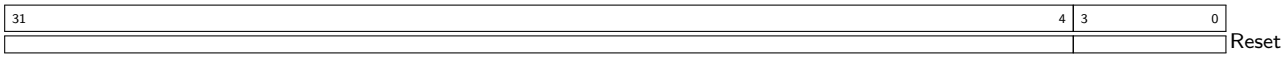
IV


31
1
0
Reset

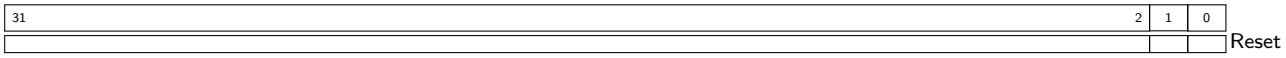

31
1
0
Reset

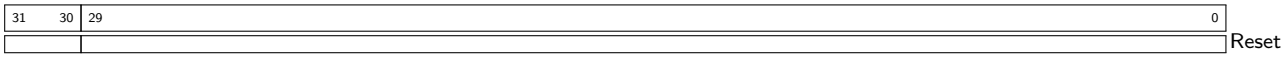

31
1
0
Reset


31
1
0
Reset

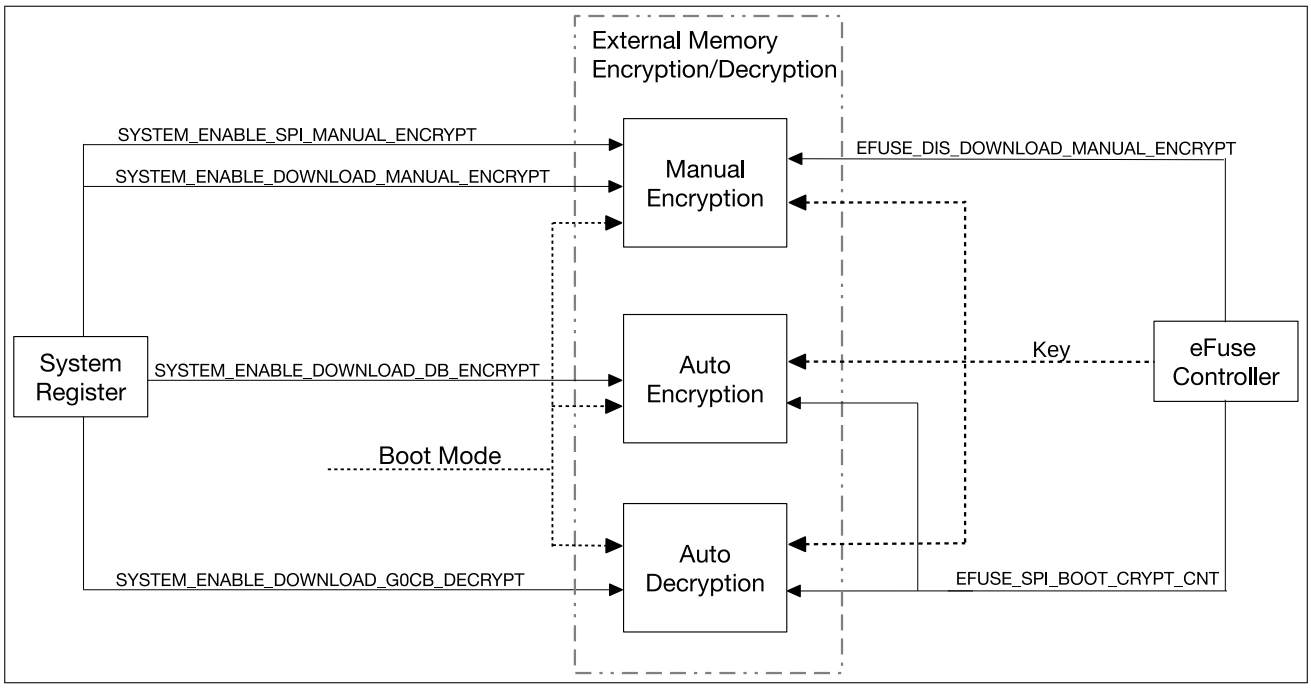

31
4
3
0
Reset

$DSKEY$


31
2
1
0
Reset


31
30
29
0
Reset

-
-
-
-
-


External Memory
Encryption/Decryption
SYSTEM_ENABLE_SPI_MANUAL_ENCRYPT
SYSTEM_ENABLE_DOWNLOAD_MANUAL_ENCRYPT
Manual
Encryption
EFUSE_DIS_DOWNLOAD_MANUAL_ENCRYPT
System
Register
SYSTEM_ENABLE_DOWNLOAD_DB_ENCRYPT
Auto
Encryption
Key
eFuse
Controller
Boot Mode
Auto
Decryption
SYSTEM_ENABLE_DOWNLOAD_G0CB_DECRYPT
EFUSE_SPI_BOOT_CRYPT_CNT

-
-
-
-

$KeyKey$

$KeyKey$

- ${}_{AA}Key_A$
- ${}_{BB}Key_B$
- ${}_{CC}Key_C$

$Key_{ABC}Key_{ABC}$

$KeyKey_AKey_BKey_C$

A	B	C	Key	Key
			$Key_A \| \| Key_B$	
			$Key_A \| \| 0^{256}$	
			$0^{256} \| \| Key_B$	
			Key_C	
			0^{256}	

$0^{256}||$

- $type$
- $size$
- $baseaddrsizebaseaddrsize == 0$

$tweaktweaktype * 2^{30}baseaddrtweak$

$addressoffset = address64n\frac{offset}{4}n$

$sizeoffset$

$offset$		$offset$	

$offset$		$offset$	

-
-

- Key

-
-

- Key
-

-

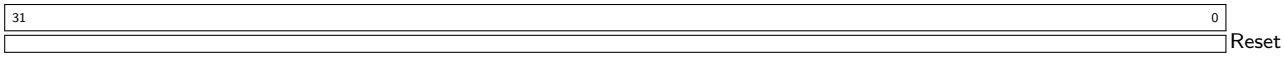
-

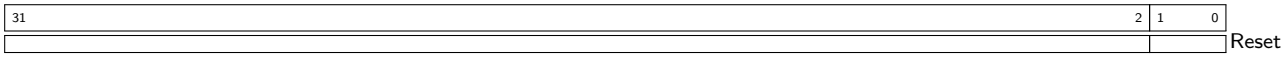
- Key
-

  - $type$
  - $baseaddr$
  - $\frac{size}{32}$

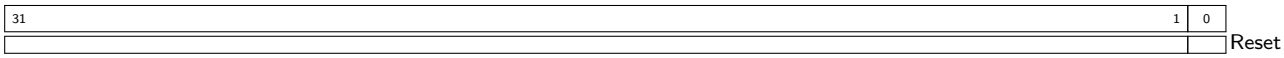
  $typebaseaddrsize$

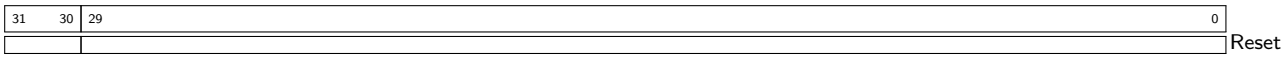
  Key

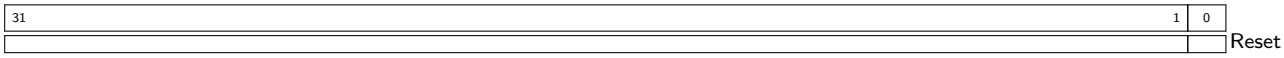

31
0
Reset

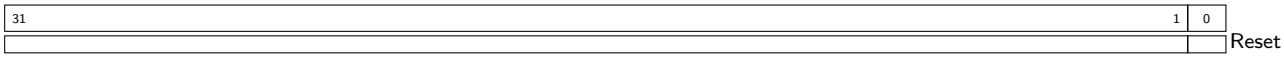

31
2
1
0
Reset

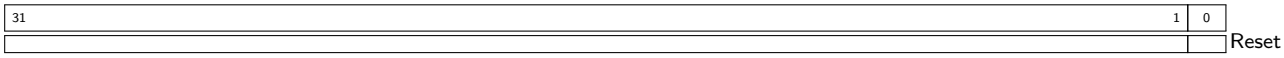
-
-
-

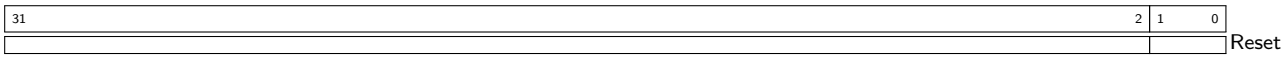

31
1
0
Reset


31
30
29
0
Reset

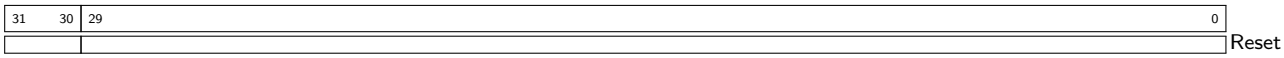

31
1
0
Reset

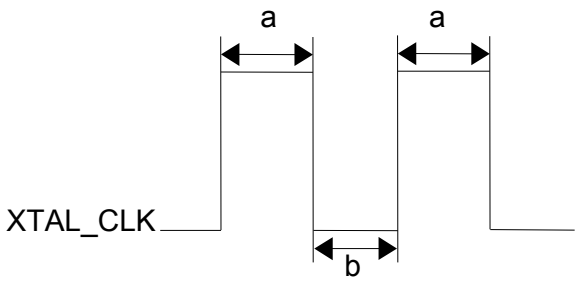

31
1
0
Reset

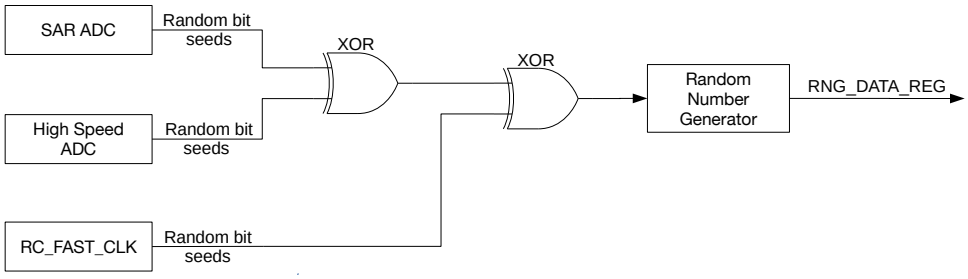

31
1
0
Reset


31
2
1
0
Reset

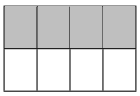
-
-
-
-

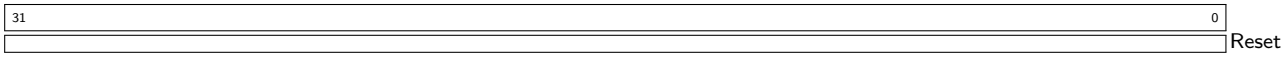

31
30
29
0
Reset

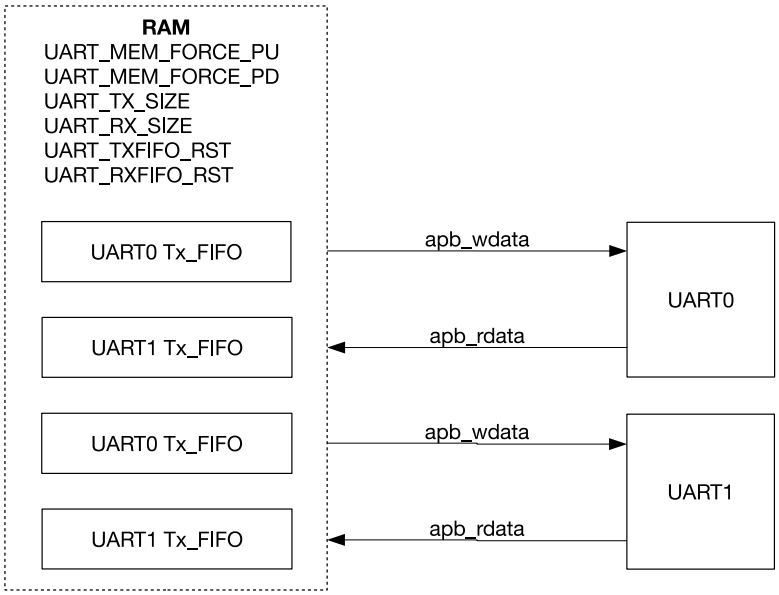

a
a
XTAL_CLK
b

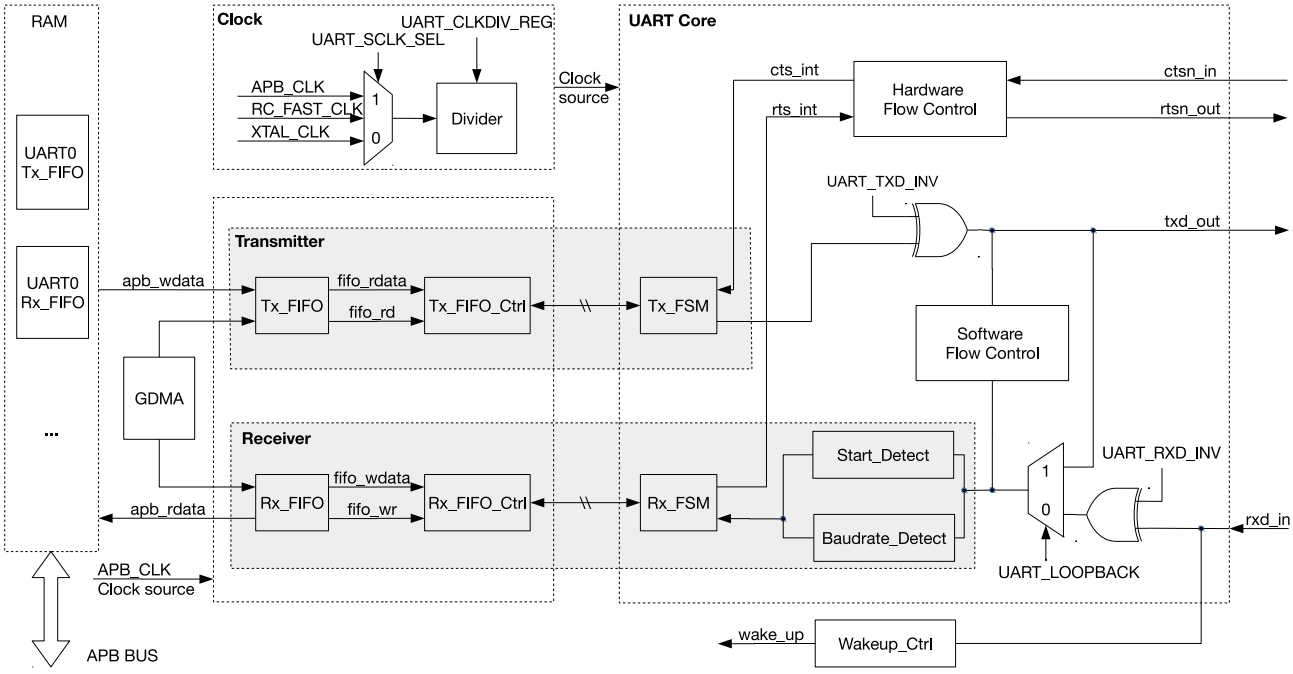

SAR ADC
Random bit seeds
High Speed ADC
Random bit seeds
RC_FAST_CLK
Random bit seeds
XOR
XOR
Random Number Generator
RNG_DATA_REG

-
-
-

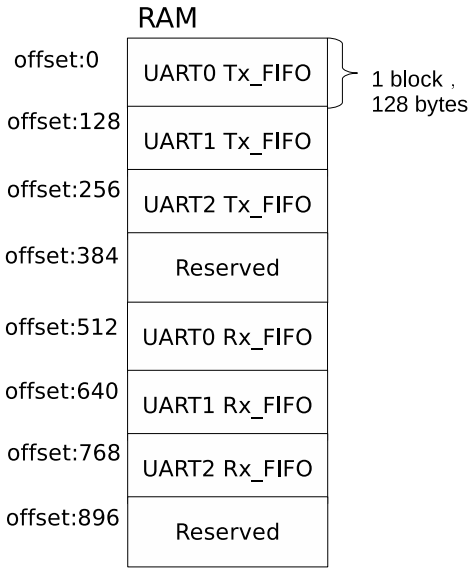



31
0
Reset


RAM
UART_MEM_FORCE_PU
UART_MEM_FORCE_PD
UART_TX_SIZE
UART_RX_SIZE
UART_TXFIFO_RST
UART_RXFIFO_RST
UART0 Tx_FIFO
UART1 Tx_FIFO
UART0 Tx_FIFO
UART1 Tx_FIFO
apb_wdata
apb_rdata
apb_wdata
apb_rdata
UART0
UART1


RAM
UART0 Tx_FIFO
UART0 Rx_FIFO
...
GDMA
APB_CLK
Clock source
APB BUS
Clock
UART_CLKDIV_REG
UART_SCLK_SEL
APB_CLK
RC_FAST_CLK
XTAL_CLK
Divider
Clock source
UART Core
Transmitter
apb_wdata
Tx_FIFO
fifo_rdata
fifo_rd
Tx_FIFO_Ctrl
Tx_FSM
Receiver
apb_rdata
Rx_FIFO
fifo_wdata
fifo_wr
Rx_FIFO_Ctrl
Rx_FSM
cts_int
rts_int
Hardware Flow Control
ctsn_in
rtsn_out
UART_TXD_INV
txd_out
Software Flow Control
Start_Detect
Baudrate_Detect
UART_RXD_INV
rxd_in
UART_LOOPBACK
wake_up
Wakeup_Ctrl

$$UARTSCLKDIVNUM + \frac{UARTSCLKDIVB}{UARTSCLKDIVA}$$

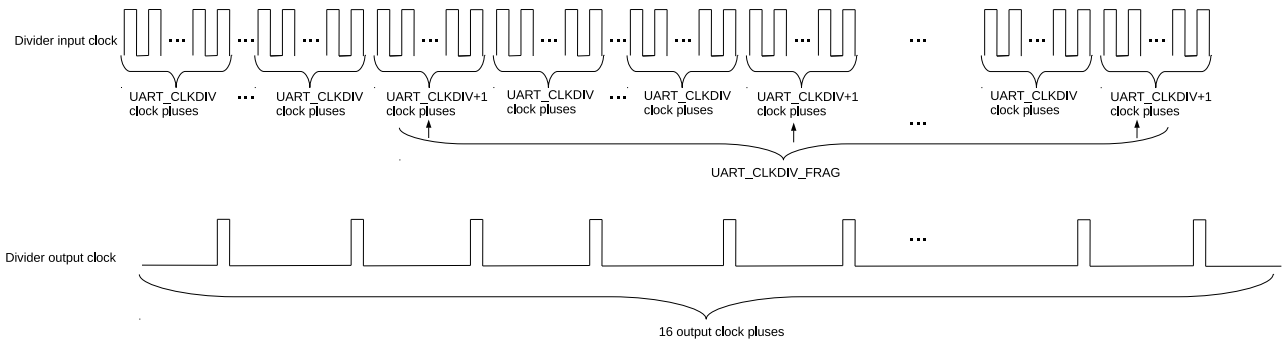


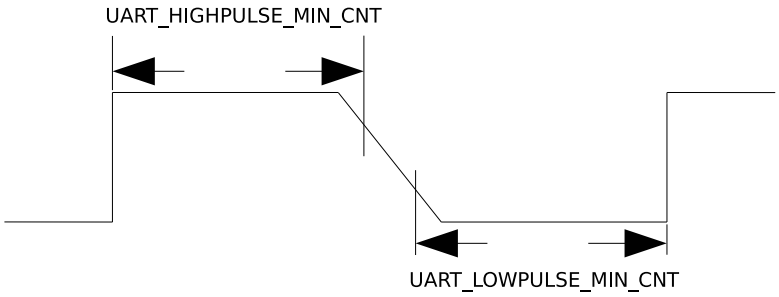
-
-
-
-
-
-

$$UARTCLKDIV + \frac{UARTCLKDIVFRAG}{16}$$

$$\frac{INPUTFREQ}{UARTCLKDIV + \frac{UARTCLKDIVFRAG}{16}}$$

$$694 + \frac{7}{16} = 694.4375$$

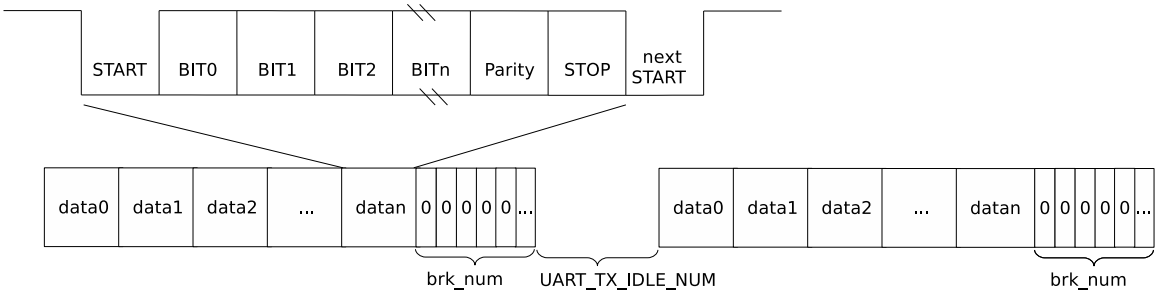


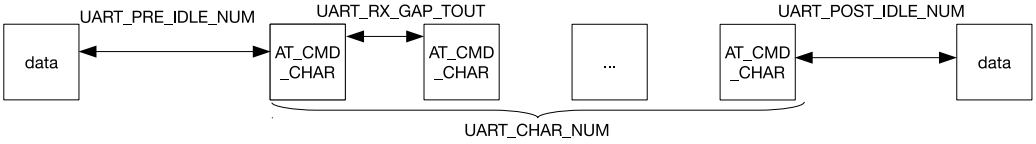


$$B = \frac{f}{}$$

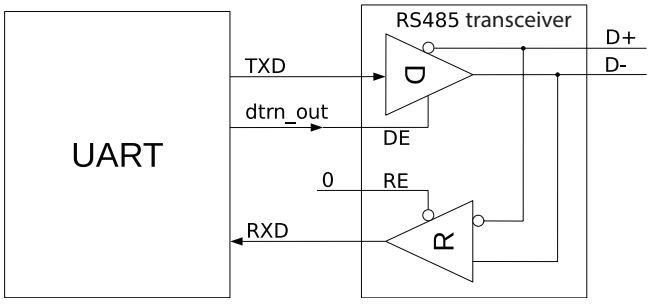
$$B = \frac{f}{}$$

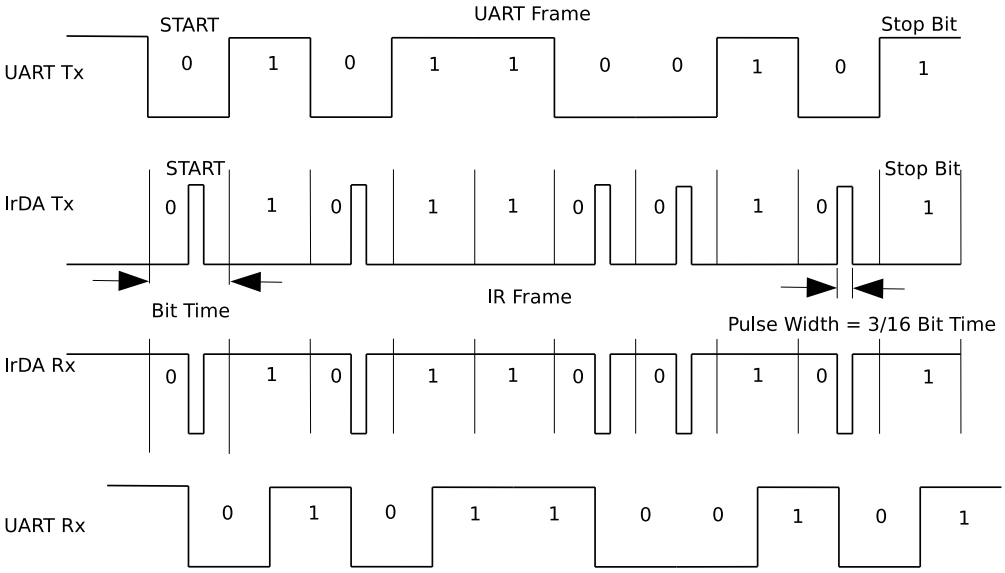
$$B = \frac{f}{}$$

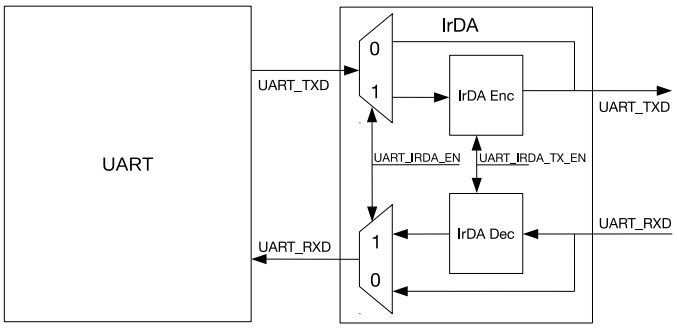


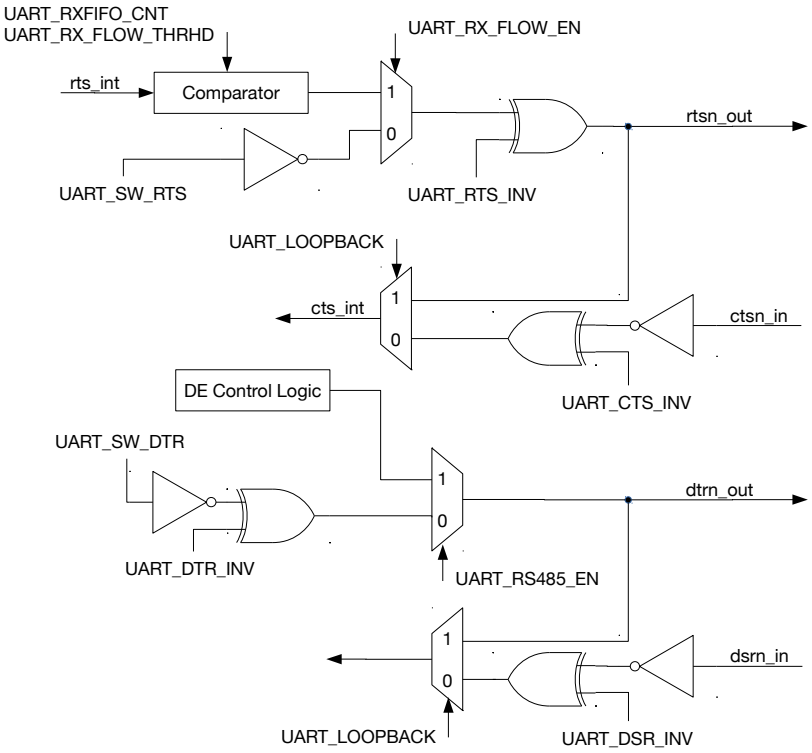

UART_PRE_IDLE_NUM
UART_RX_GAP_TOUT
UART_POST_IDLE_NUM
data
AT_CMD
_CHAR
AT_CMD
_CHAR
...
AT_CMD
_CHAR
data
UART_CHAR_NUM

-
-
-
-

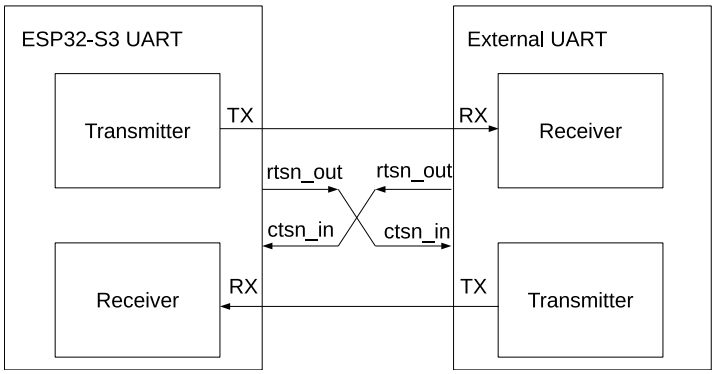

UART
TXD
dtrn_out
0
RXD
RS485 transceiver
D
DE
RE
R
D+
D-

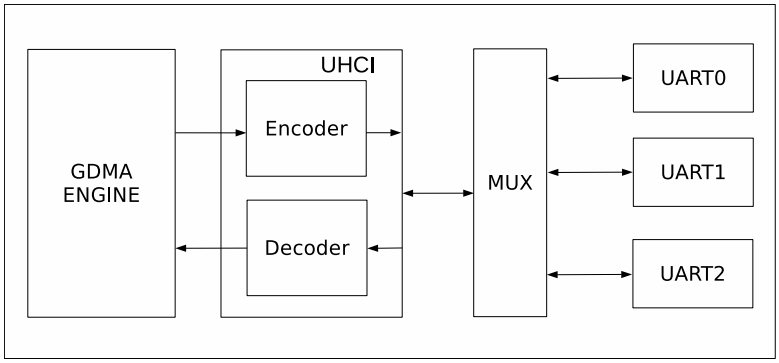

START
UART Frame
Stop Bit
UART Tx
0 1 0 1 1 0 0 1 0 1
START
Stop Bit
IrDA Tx
0 1 0 1 1 0 0 1 0 1
Bit Time
IR Frame
Pulse Width = 3/16 Bit Time
IrDA Rx
0 1 0 1 1 0 0 1 0 1
UART Rx
0 1 0 1 1 0 0 1 0 1


UART
UART_TXD
UART_RXD
IrDA
0
1
IrDA Enc
UART_TXD
UART_IRDA_EN
UART_IRDA_TX_EN
IrDA Dec
UART_RXD
1
0


UART_RXFIFO_CNT
UART_RX_FLOW_THRHD
UART_RX_FLOW_EN
rts_int
Comparator
1
0
rtsn_out
UART_SW_RTS
UART_RTS_INV
UART_LOOPBACK
cts_int
1
0
ctsn_in
UART_CTS_INV
DE Control Logic
UART_SW_DTR
1
0
dtrn_out
UART_DTR_INV
UART_RS485_EN
1
0
dsrn_in
UART_LOOPBACK
UART_DSR_INV

-
-


ESP32-S3 UART
External UART
Transmitter
TX
RX
Receiver
rtsn_out
rtsn_out
ctsn_in
ctsn_in
Receiver
RX
TX
Transmitter


UHCI
Encoder
Decoder
GDMA
ENGINE
MUX
UART0
UART1
UART2

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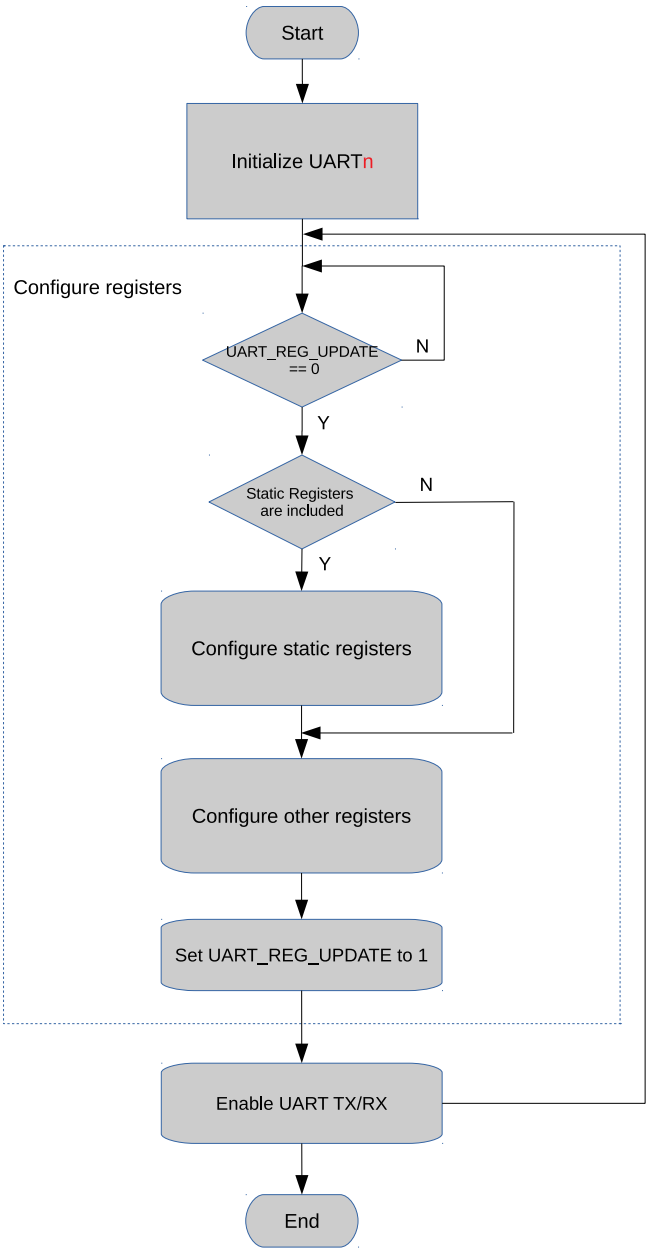
Start
Initialize UARTn
Configure registers
UART_REG_UPDATE == 0
N
Y
Static Registers are included
N
Y
Configure static registers
Configure other registers
Set UART_REG_UPDATE to 1
Enable UART TX/RX
End

-
-
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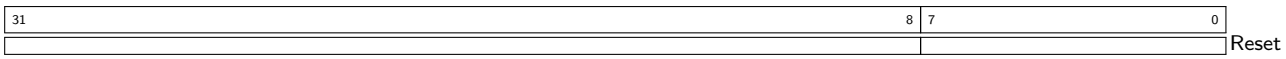
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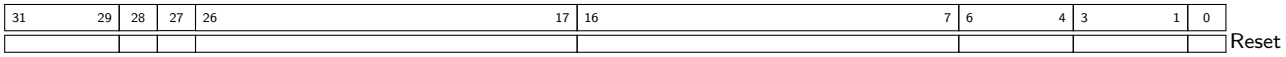
Reset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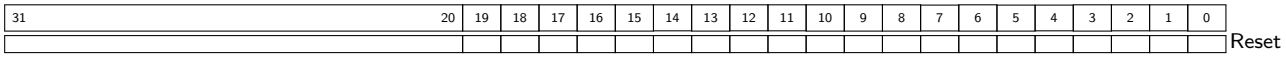
Reset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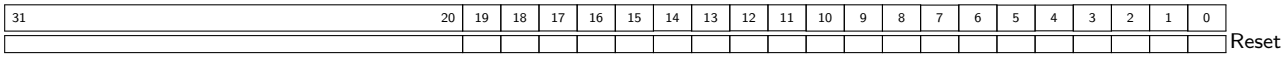
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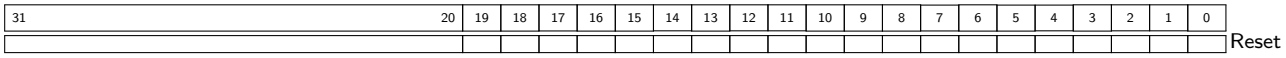
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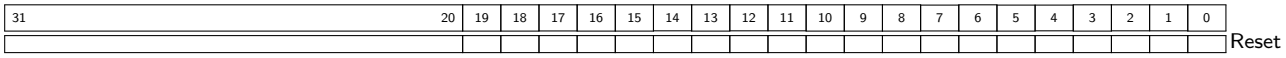
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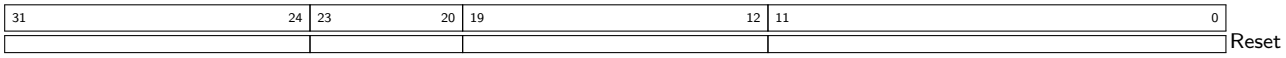
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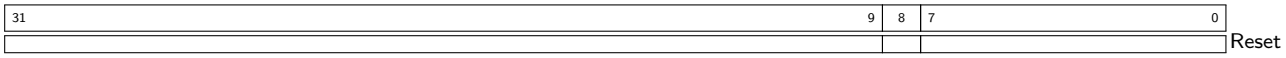
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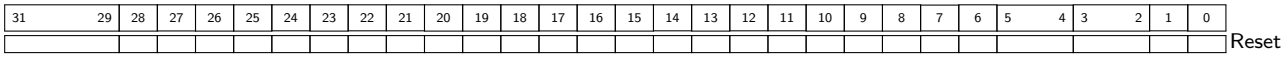
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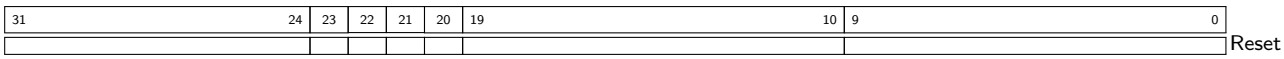
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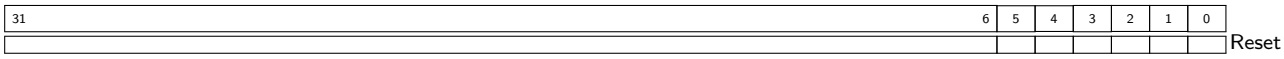
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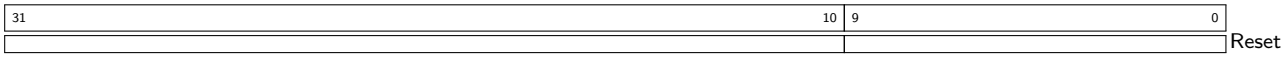
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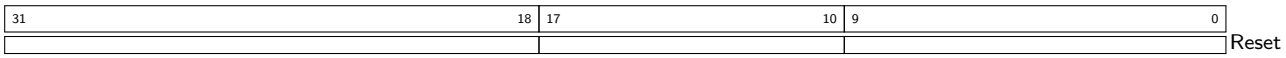
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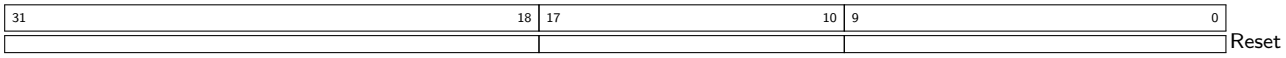
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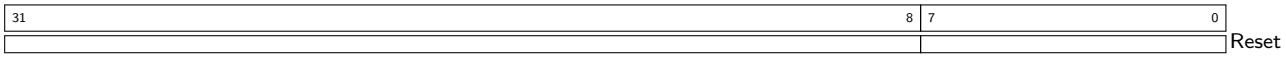
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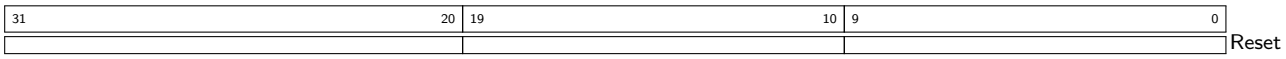
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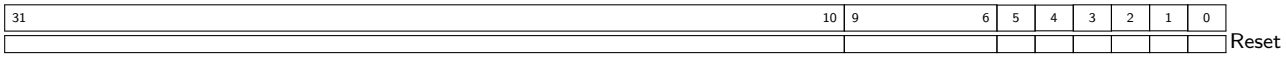
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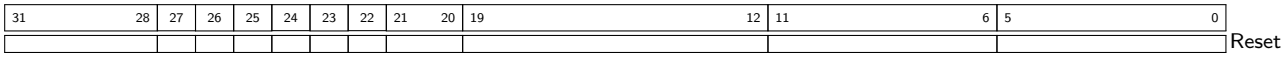
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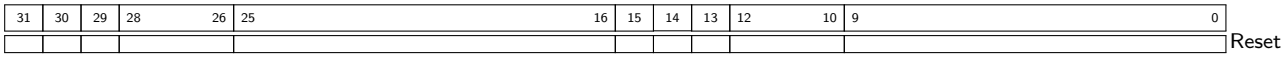
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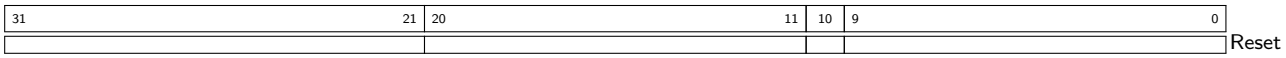
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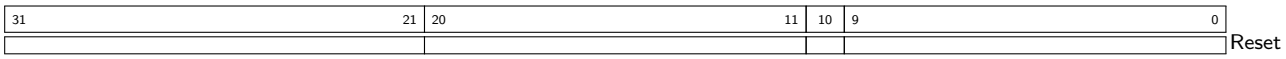
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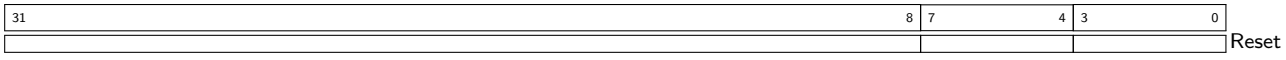
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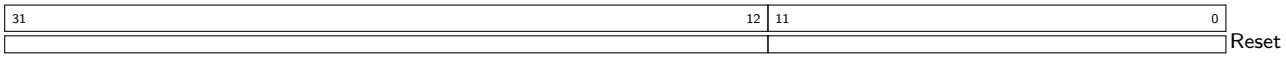
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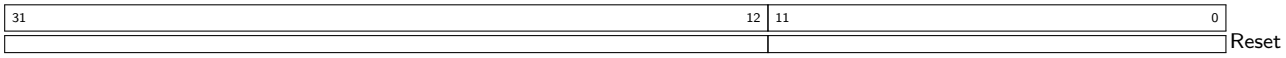
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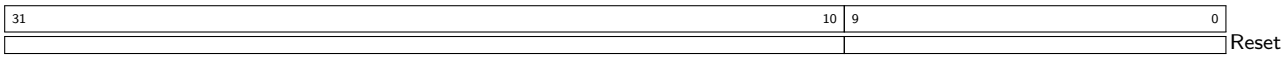
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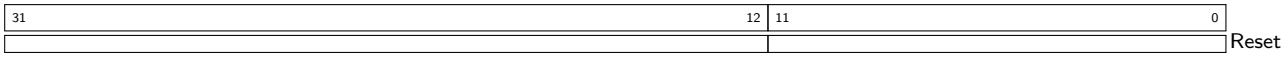
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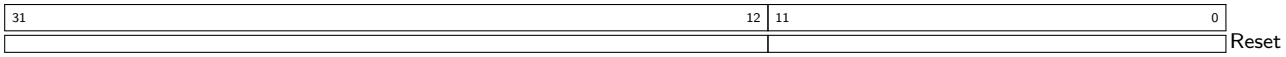
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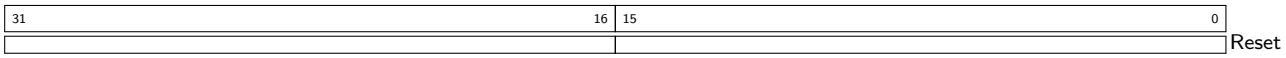
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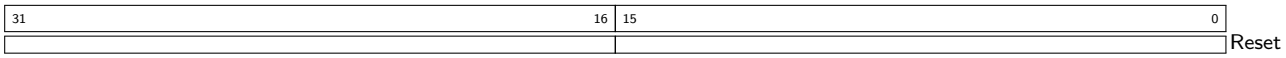
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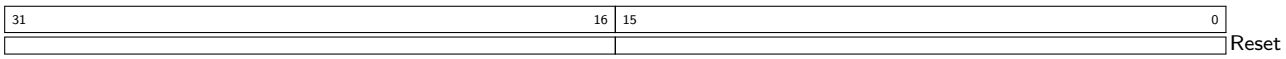
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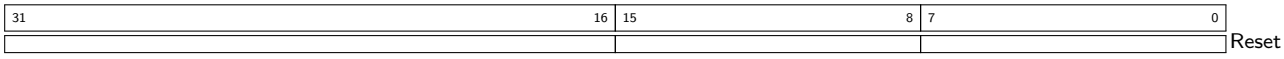
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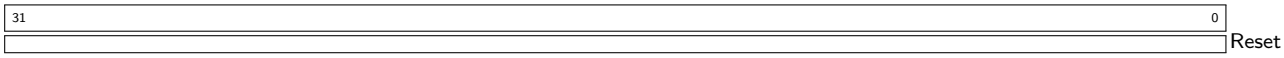
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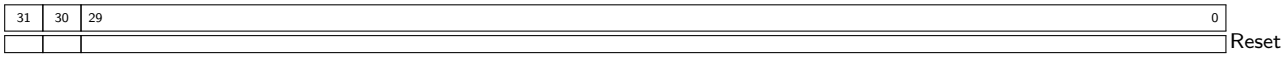
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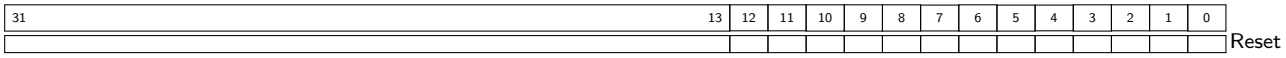
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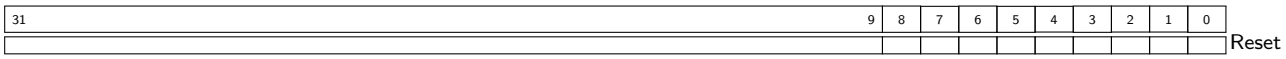
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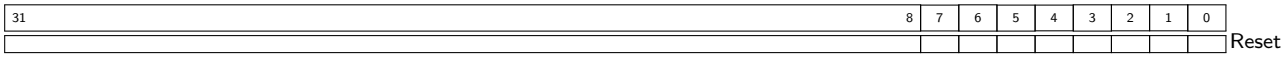
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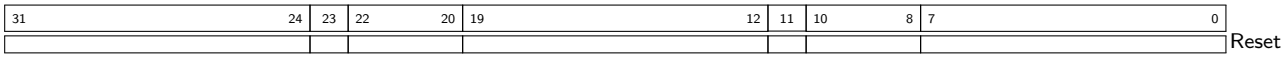
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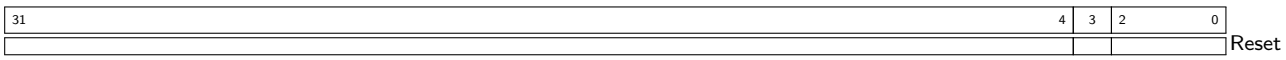
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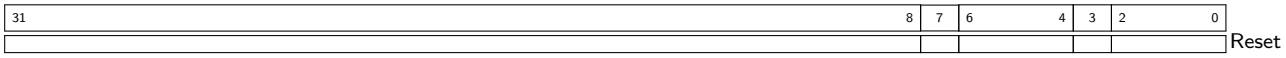
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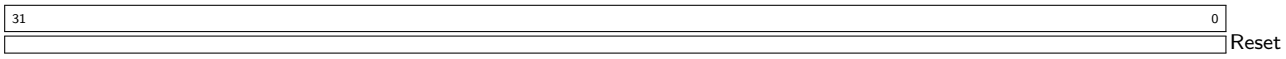
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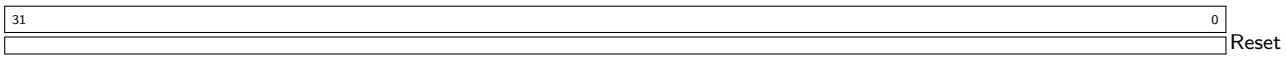
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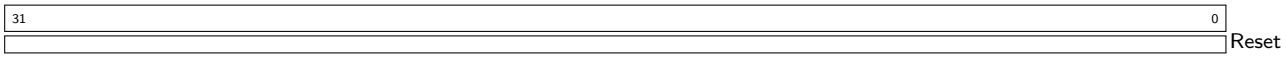
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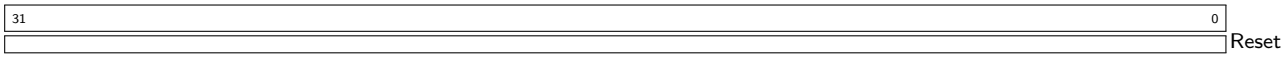
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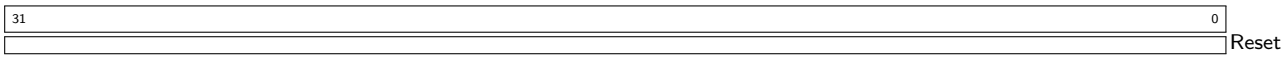
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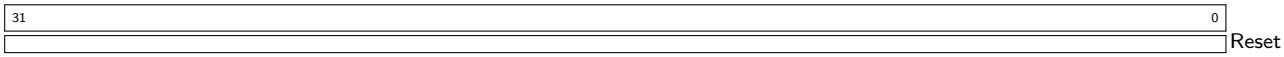
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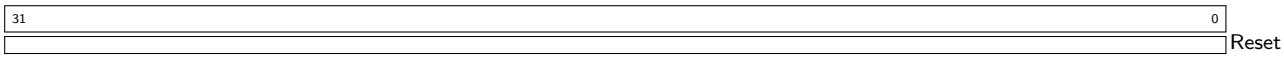
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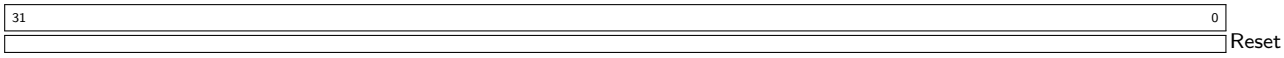
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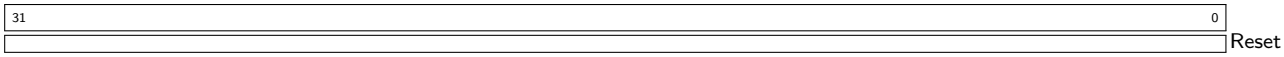
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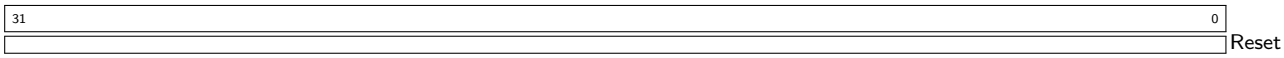
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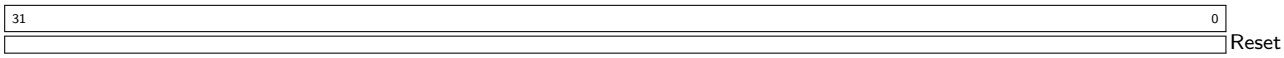
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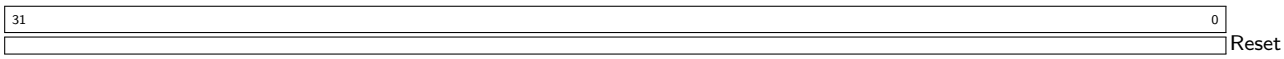
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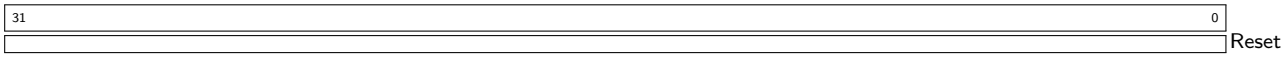
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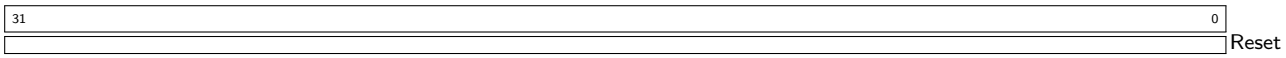
Reset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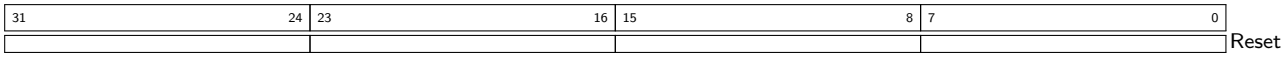
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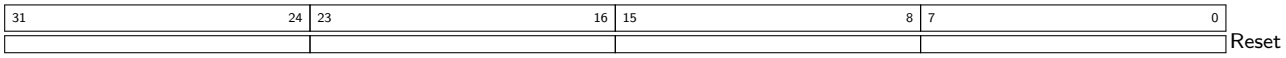
23
16
15
8
7
0
Reset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24
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16
15
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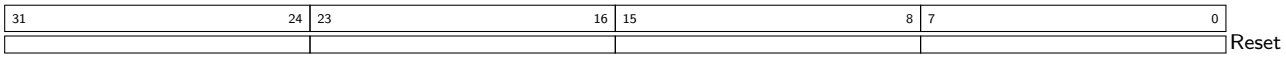
Reset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23
16
15
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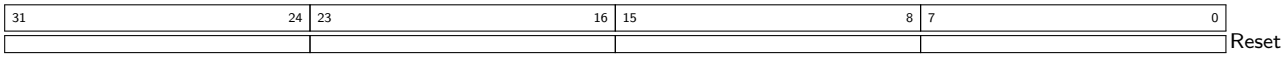
Reset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16
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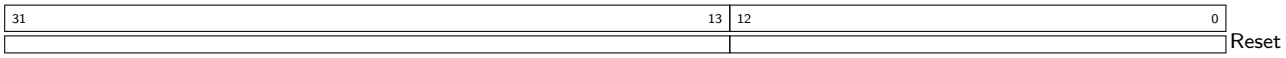
Reset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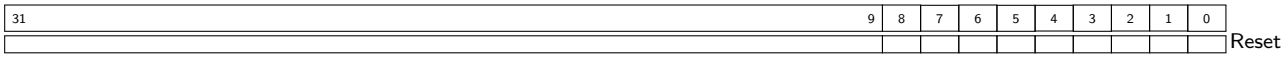
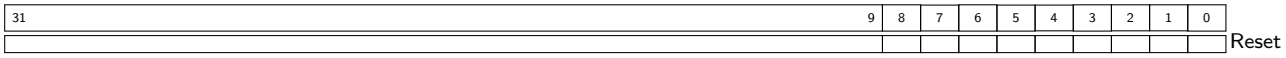

31
9
8
7
6
5
4
3
2
1
0
Reset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8
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6
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2
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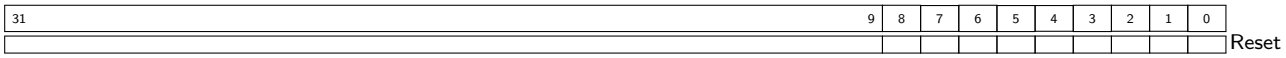
Reset


31
9
8
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5
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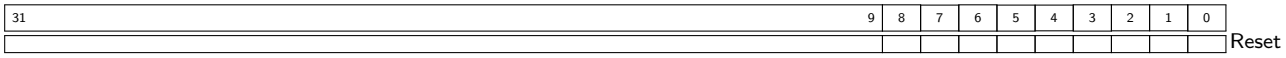
3
2
1
0
Reset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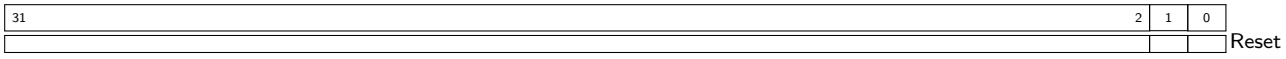
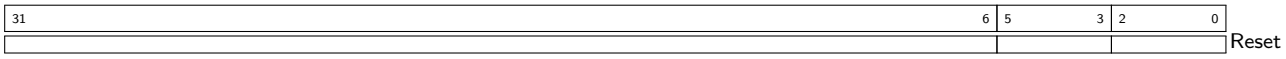
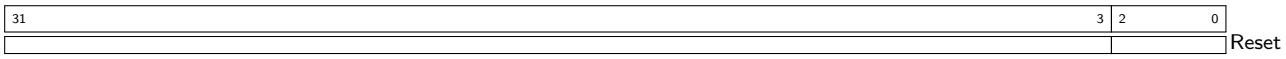
9
8
7
6
5
4
3
2
1
0
Reset


31
2
1
0
Reset


31
6
5
3
2
0
Reset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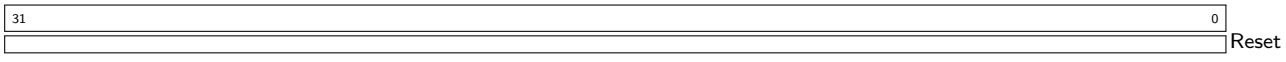
3
2
0
Reset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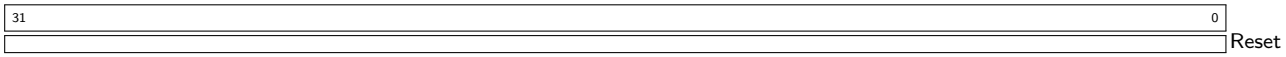
31
0
Reset

$R/\overline{W}R/\overline{W}R/\overline{W}$

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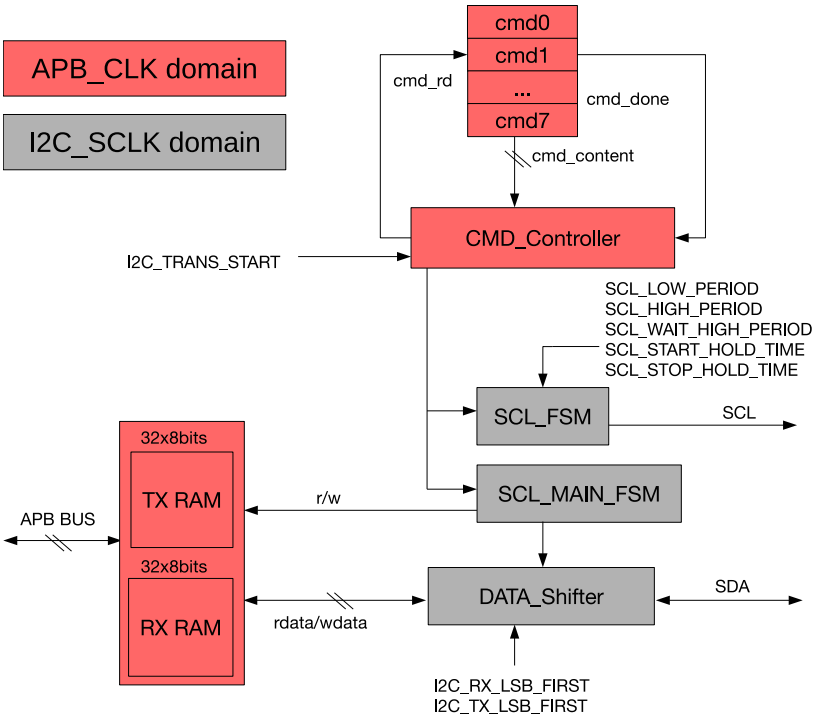
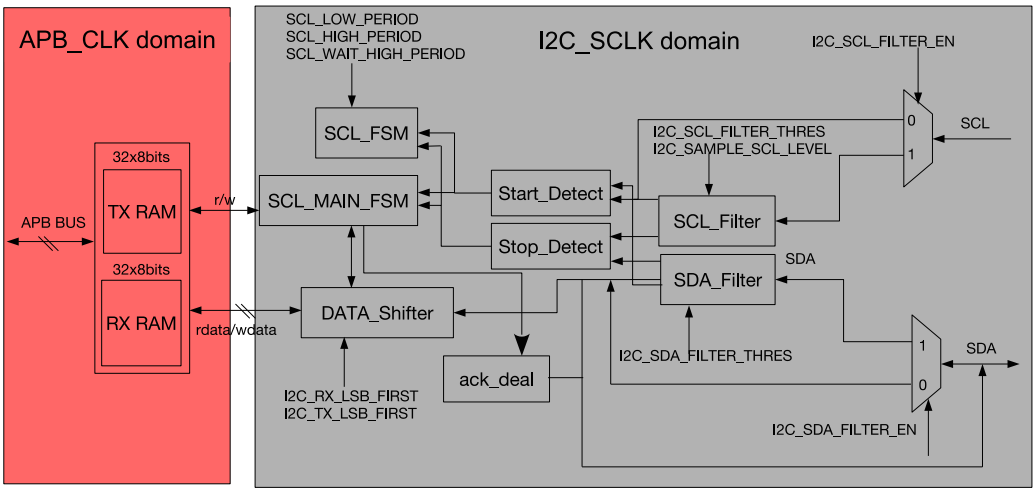

APB_CLK domain
I2C_SCLK domain
cmd0
cmd1
...
cmd7
cmd_rd
cmd_done
cmd_content
CMD_Controller
I2C_TRANS_START
SCL_LOW_PERIOD
SCL_HIGH_PERIOD
SCL_WAIT_HIGH_PERIOD
SCL_START_HOLD_TIME
SCL_STOP_HOLD_TIME
SCL_FSM
SCL
32x8bits
TX RAM
r/w
SCL_MAIN_FSM
APB BUS
32x8bits
RX RAM
rdata/wdata
DATA_Shifter
SDA
I2C_RX_LSB_FIRST
I2C_TX_LSB_FIRST


APB_CLK domain
I2C_SCLK domain
SCL_LOW_PERIOD
SCL_HIGH_PERIOD
SCL_WAIT_HIGH_PERIOD
I2C_SCL_FILTER_EN
SCL_FSM
I2C_SCL_FILTER_THRES
I2C_SAMPLE_SCL_LEVEL
SCL
32x8bits
TX RAM
r/w
SCL_MAIN_FSM
Start_Detect
SCL_Filter
APB BUS
Stop_Detect
SDA
32x8bits
RX RAM
SDA_Filter
DATA_Shifter
rdata/wdata
I2C_SDA_FILTER_THRES
SDA
ack_deal
I2C_RX_LSB_FIRST
I2C_TX_LSB_FIRST
I2C_SDA_FILTER_EN

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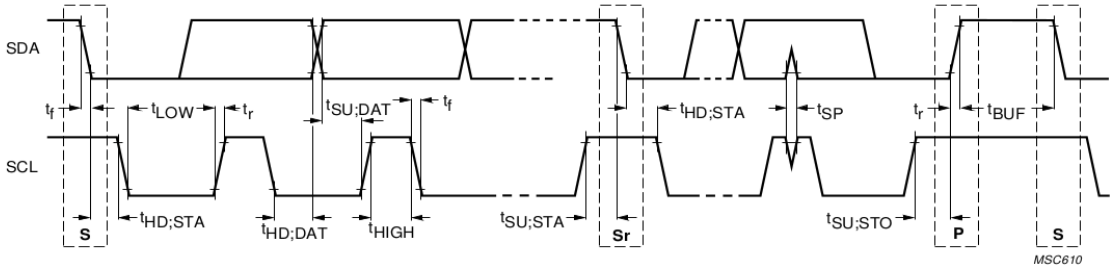

Fig.31 Definition of timing for F/S-mode devices on the I²C-bus.

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6	–	µs
LOW period of the SCL clock	t_{LOW}	4.7	–	1.3	–	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	µs
Data hold time: for CBUS compatible masters (see NOTE, Section 10.1.3) for I²C-bus devices	$t_{HD;DAT}$	 5.0 0(2)	 – 3.45(3)	 – 0(2)	 – 0.9(3)	 µs µs
Data set-up time	$t_{SU;DAT}$	250	–	100(4)	–	ns
Rise time of both SDA and SCL signals	t_r	–	1000	$20 + 0.1C_b$(5)	300	ns
Fall time of both SDA and SCL signals	t_f	–	300	$20 + 0.1C_b$(5)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	–	0.6	–	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	µs

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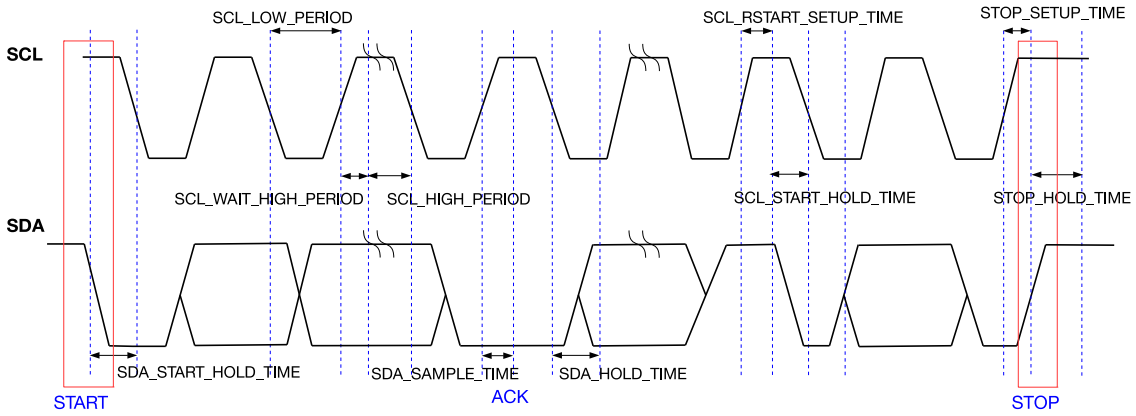
$$Divisor = I2CSCLKDIVNUM + 1 + \frac{I2CSCLKDIVA}{I2CSCLKDIVB}$$

$R/\overline{W}$



$$t_{LOW} = (I2CSCLLOWPERIOD + 1) \cdot T_{I2CSCLK}$$

$$t_{HIGH} = (I2CSCLHIGHPERIOD + 1) \cdot T_{I2CSCLK}$$

$$t_{SU:STA} = (I2CSCLRSTARTSETUPTIME + 1) \cdot T_{I2CSCLK}$$

$$t_{HD:STA} = (I2CSCLSTARTHOLDTIME + 1) \cdot T_{I2CSCLK}$$

$$t_r = (I2CSCLWAITHIGHPERIOD + 1) \cdot T_{I2CSCLK}$$

$$t_{SU:STO} = (I2CSCLSTOPSETUPTIME + 1) \cdot T_{I2CSCLK}$$

$$t_{BUF} = (I2CSCLSTOPHOLDTIME + 1) \cdot T_{I2CSCLK}$$

$$t_{HD:DAT} = (I2CSDAHOLDTIME + 1) \cdot T_{I2CSCLK}$$

$$t_{SU:DAT} = (I2CSCLLOWPERIOD - I2CSDAHOLDTIME) \cdot T_{I2CSCLK}$$

-

$$f_{scl} = \frac{f}{}$$

-

$\frac{f_{I2CSCLK}}{f_{SCL}} > 20$

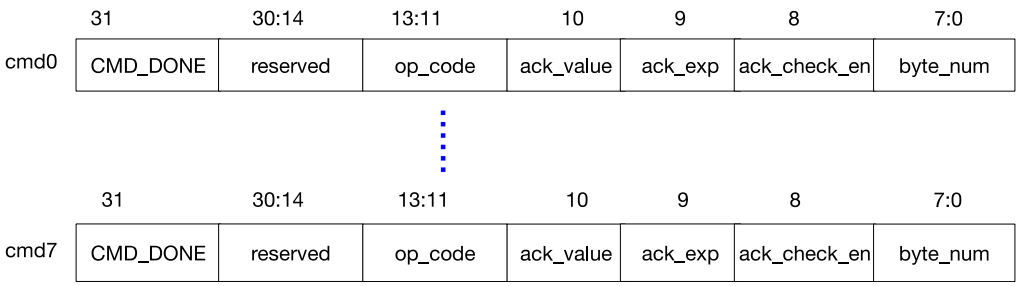
$3 \times f_{I2CSCLK} \leq (I2CSDAHOLDTIME - 4) \times f_{APBCLK}$

$I2CSCLSTTOI2C$22

$I2CSCLMAINSTTOI2C$

22

$I2CTIMEOUTVALUE$



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$R/\overline{W}R/\overline{W}$

$R/\overline{W}$

$R/\overline{W}$

$R/\overline{W}R/\overline{W}R/\overline{W}$

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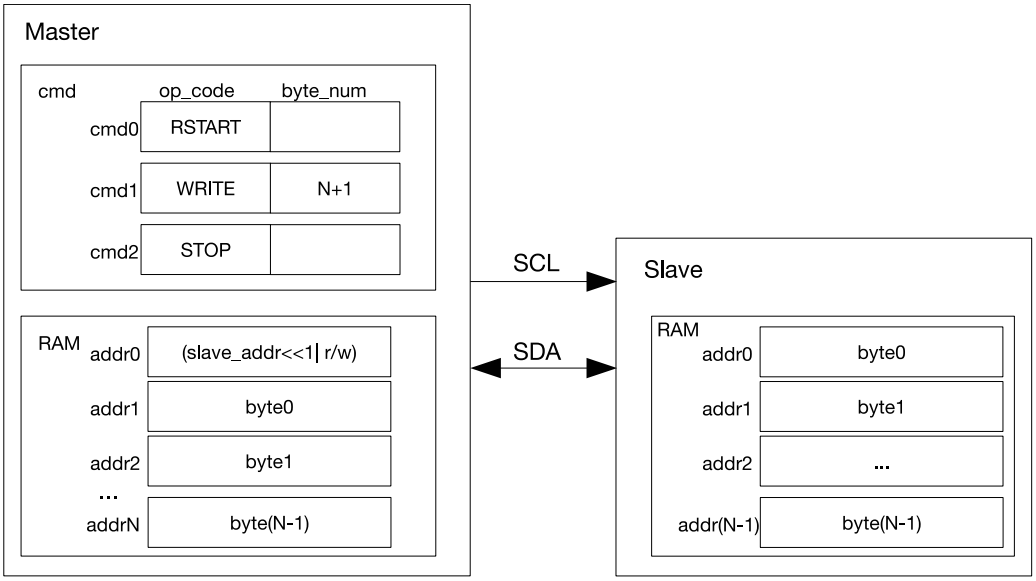

$R/\overline{W}R/\overline{W}$

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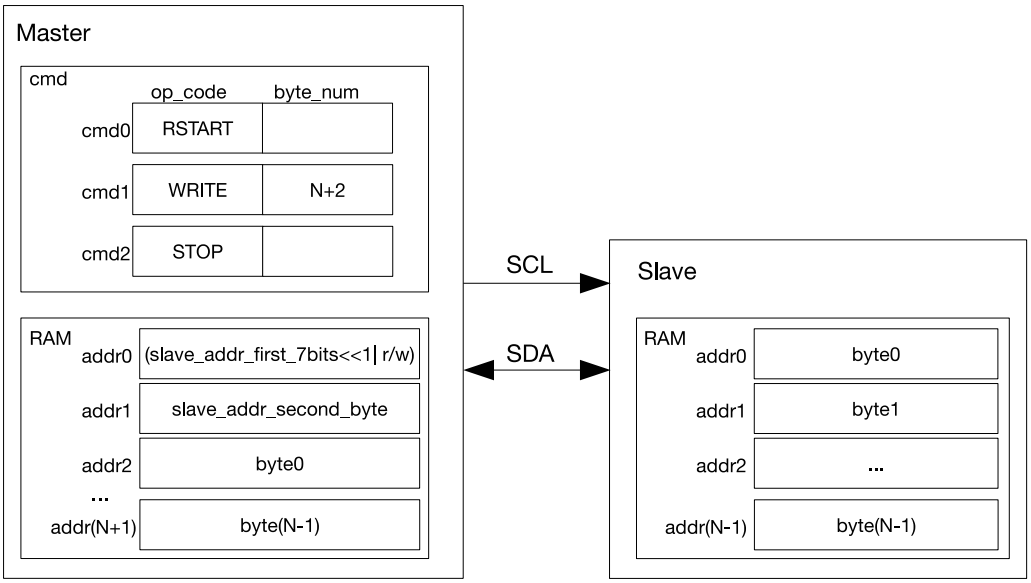
Master
cmd
op_code
byte_num
cmd0
RSTART
cmd1
WRITE
N+2
cmd2
STOP
RAM
addr0
(slave_addr_first_7bits<<1| r/w)
addr1
slave_addr_second_byte
addr2
byte0
...
addr(N+1)
byte(N-1)
SCL
SDA
Slave
RAM
addr0
byte0
addr1
byte1
addr2
...
addr(N-1)
byte(N-1)

$R/\overline{W}$

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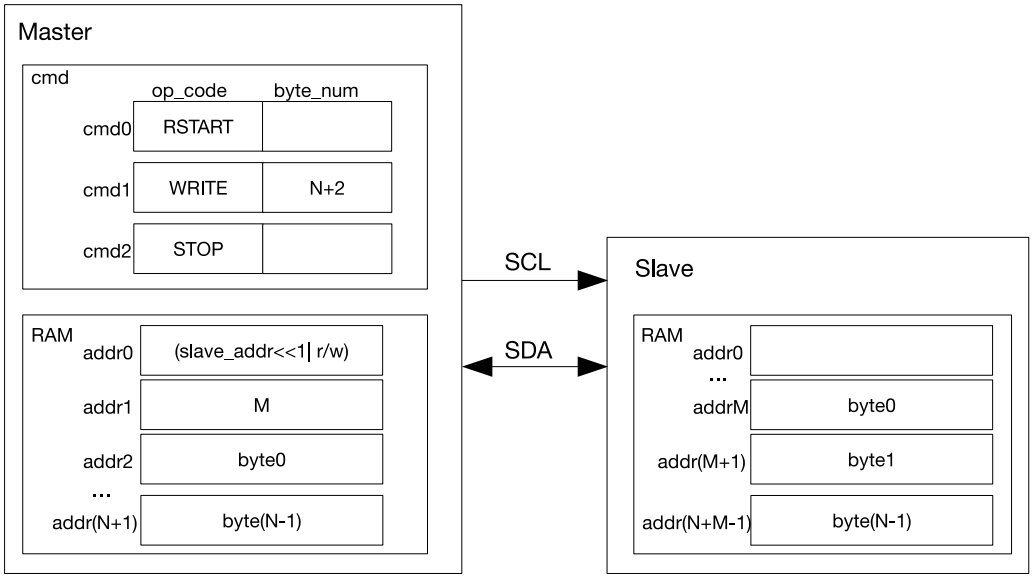
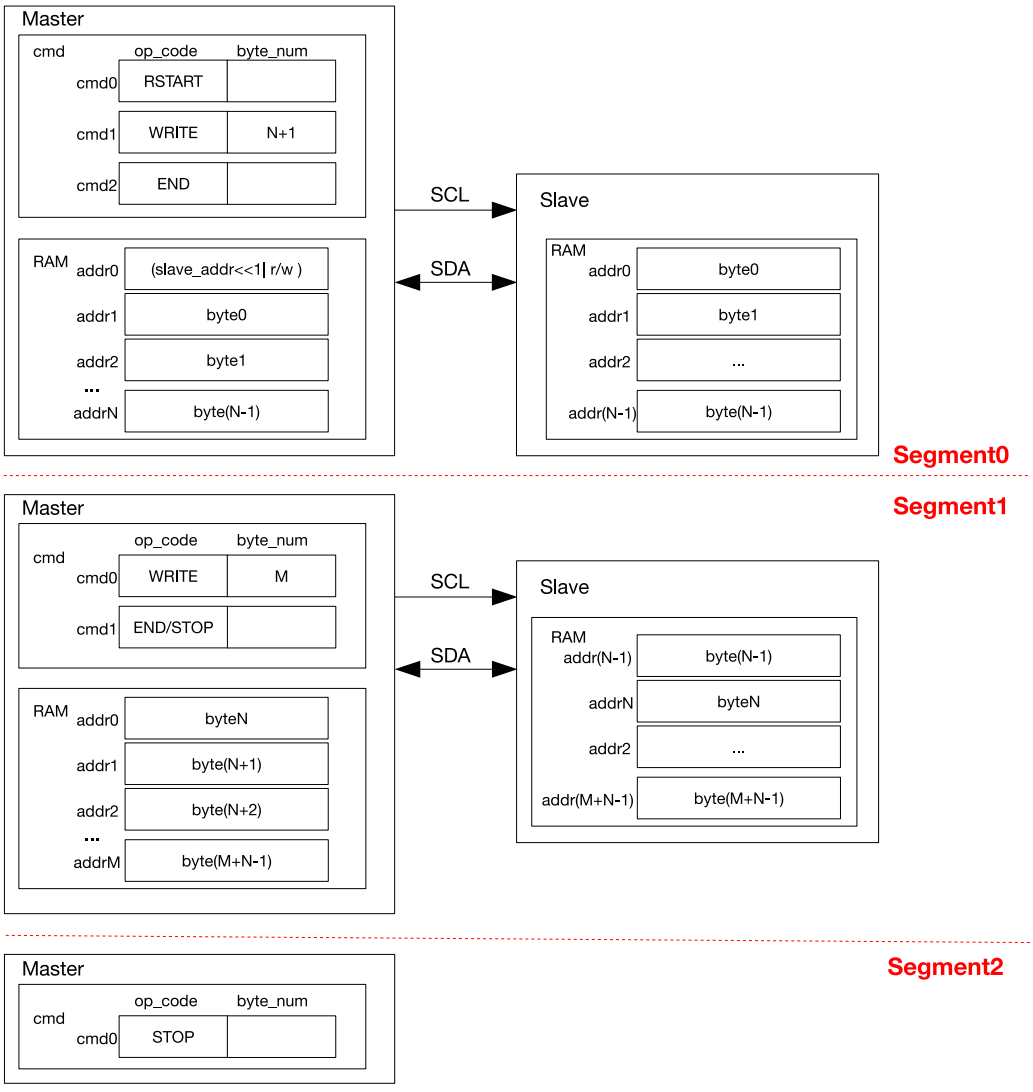
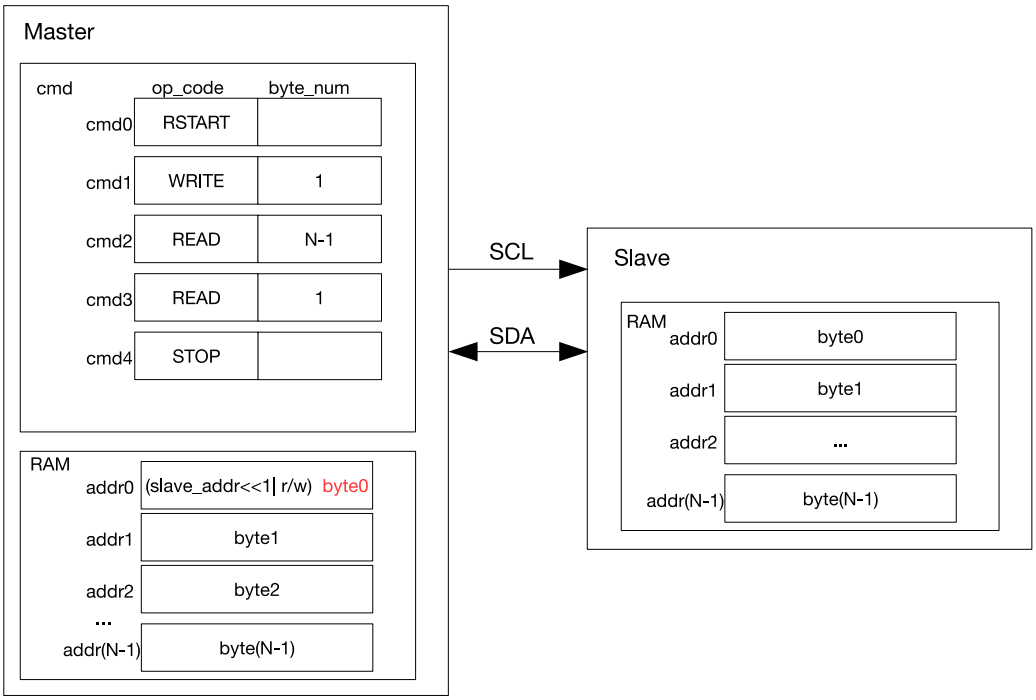
-


Master
cmd
op_code
byte_num
cmd0
RSTART
cmd1
WRITE
N+2
cmd2
STOP
RAM
addr0
(slave_addr<<1| r/w)
addr1
M
addr2
byte0
addr(N+1)
byte(N-1)
SCL
SDA
Slave
RAM
addr0
addrM
byte0
addr(M+1)
byte1
addr(N+M-1)
byte(N-1)

-
-


Master
cmd
op_code
byte_num
cmd0
RSTART
cmd1
WRITE
N+1
cmd2
END
RAM
addr0
(slave_addr<<1| r/w)
addr1
byte0
addr2
byte1
...
addrN
byte(N-1)
SCL
SDA
Slave
RAM
addr0
byte0
addr1
byte1
addr2
...
addr(N-1)
byte(N-1)
Segment0
Segment1
Master
op_code
byte_num
cmd
cmd0
WRITE
M
cmd1
END/STOP
RAM
addr0
byteN
addr1
byte(N+1)
addr2
byte(N+2)
...
addrM
byte(M+N-1)
SCL
SDA
Slave
RAM
addr(N-1)
byte(N-1)
addrN
byteN
addr2
...
addr(M+N-1)
byte(M+N-1)
Segment2
Master
op_code
byte_num
cmd
cmd0
STOP

-
-



$R/\overline{W}R/\overline{W}$

$R/\overline{W}$

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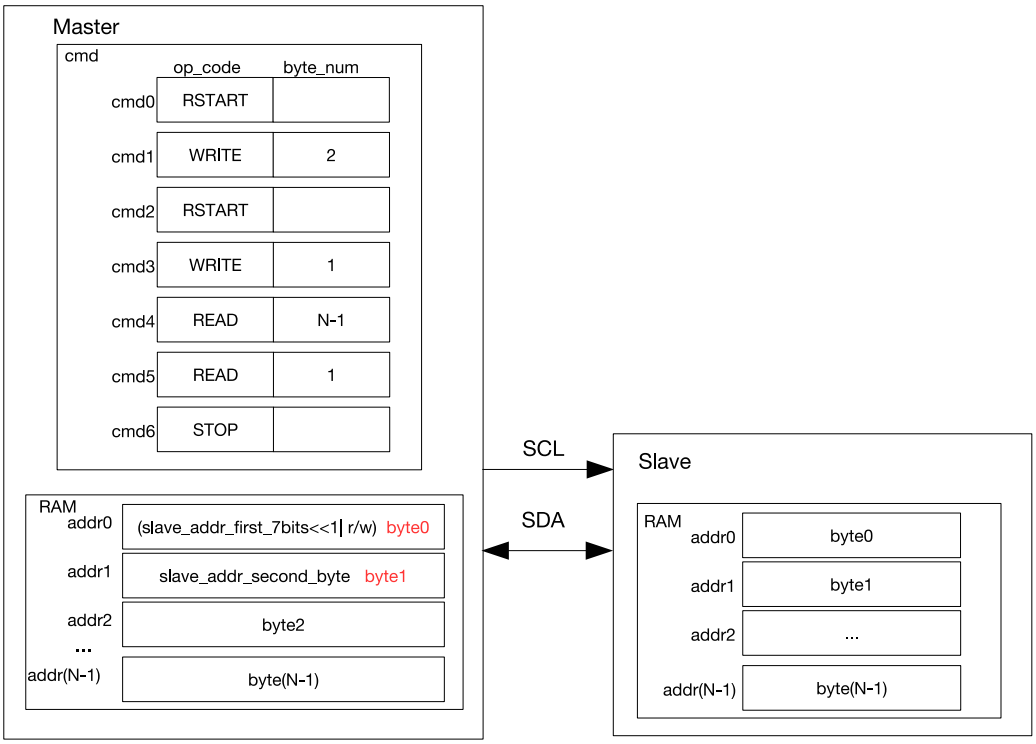

$R/\overline{W}$ $R/\overline{W}$

$R/\overline{W}\,R/\overline{W}$

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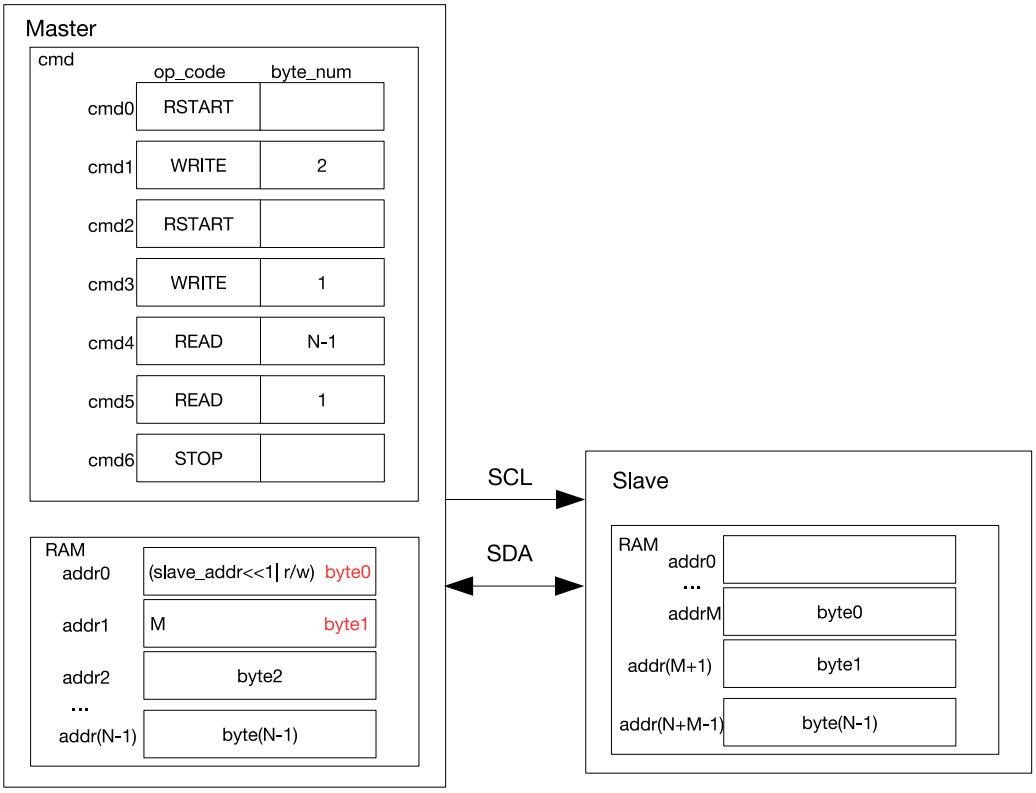
$R/\overline{W}$



$R/\overline{W}$ $R/\overline{W}$

$R/\overline{W}$ $R/\overline{W}$

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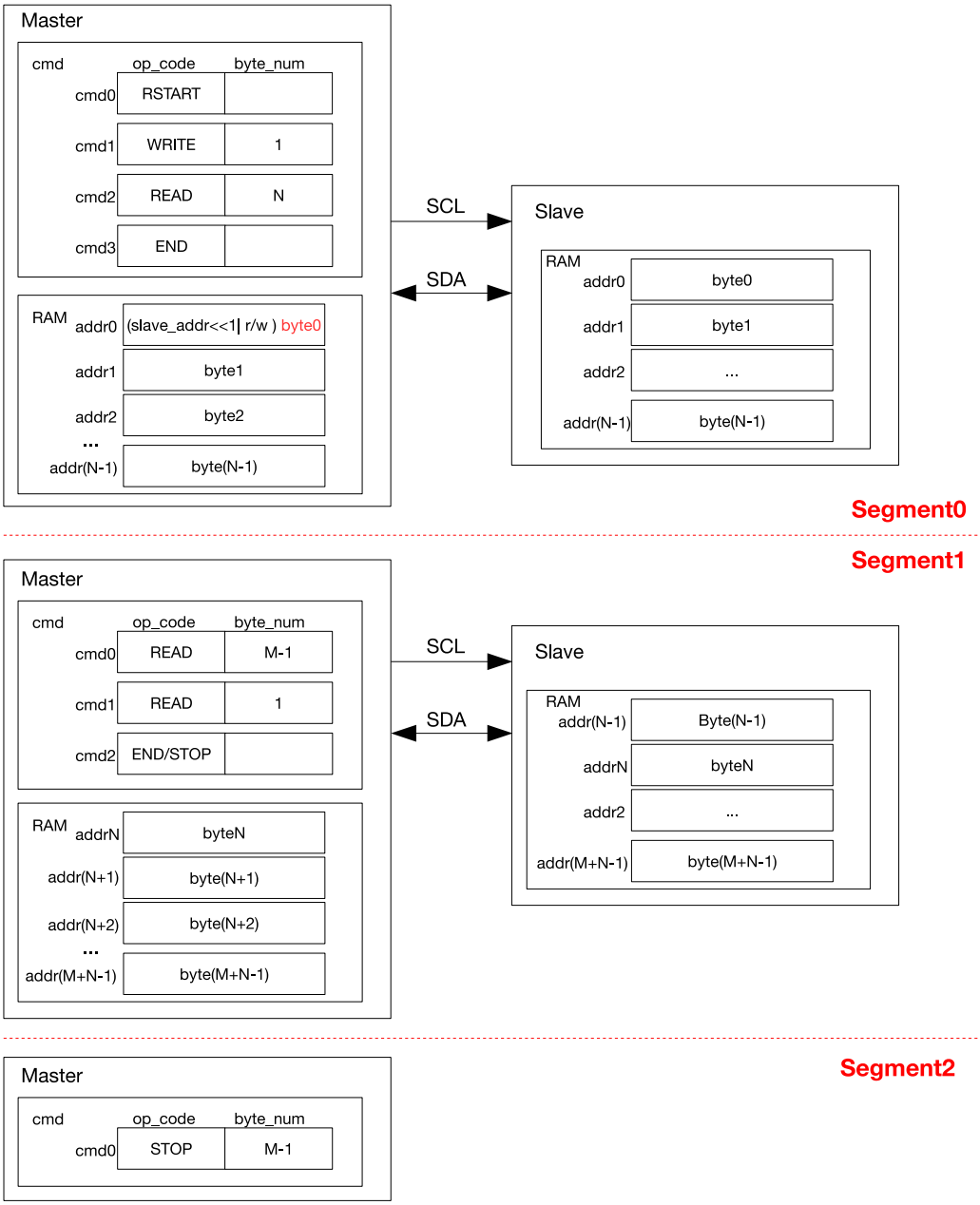
Master
cmd
op_code
byte_num
cmd0
RSTART
cmd1
WRITE
1
cmd2
READ
N
cmd3
END
RAM
addr0
(slave_addr<<1| r/w) byte0
addr1
byte1
addr2
byte2
...
addr(N-1)
byte(N-1)
SCL
SDA
Slave
RAM
addr0
byte0
addr1
byte1
addr2
...
addr(N-1)
byte(N-1)
Segment0
Segment1
Master
cmd
op_code
byte_num
cmd0
READ
M-1
cmd1
READ
1
cmd2
END/STOP
RAM
addrN
byteN
addr(N+1)
byte(N+1)
addr(N+2)
byte(N+2)
...
addr(M+N-1)
byte(M+N-1)
SCL
SDA
Slave
RAM
addr(N-1)
Byte(N-1)
addrN
byteN
addr2
...
addr(M+N-1)
byte(M+N-1)
Segment2
Master
cmd
op_code
byte_num
cmd0
STOP
M-1

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- *I2CTIMEOUTVALUE*
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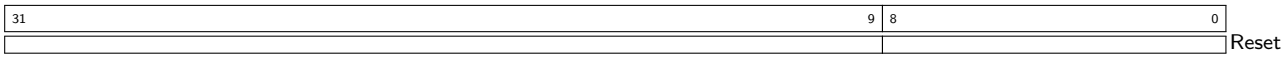
31
9
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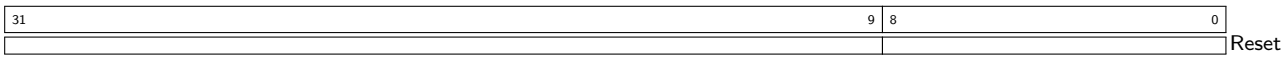
Reset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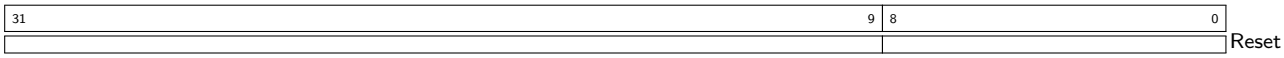
Reset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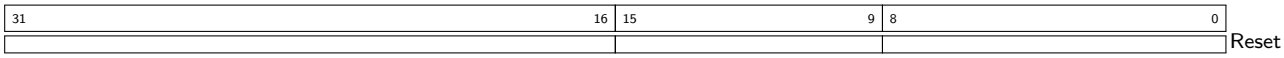
Reset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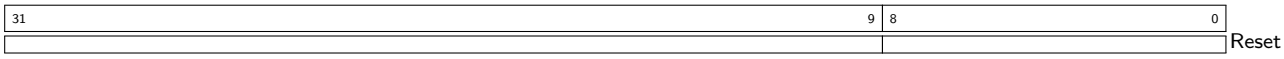
Reset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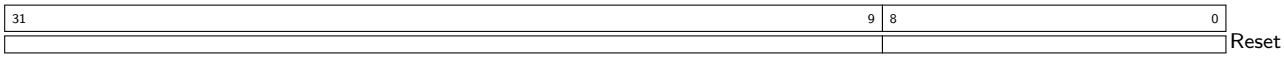
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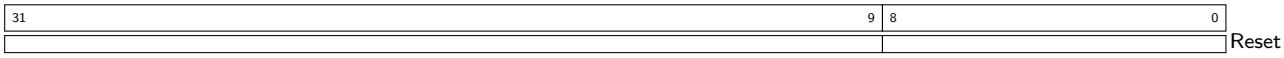
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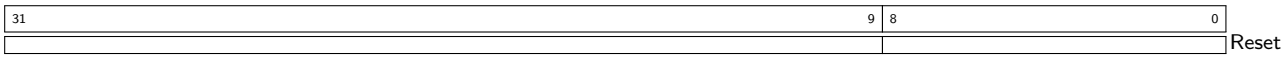
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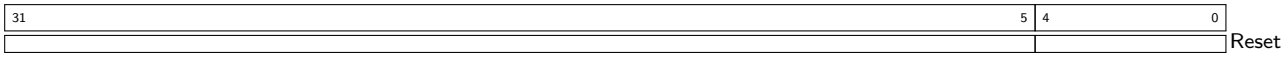
Reset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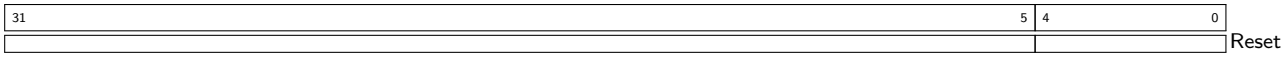
0
Reset


31
5
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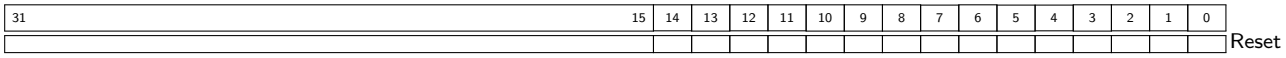
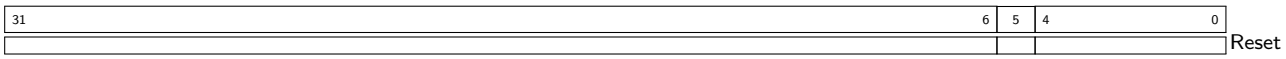
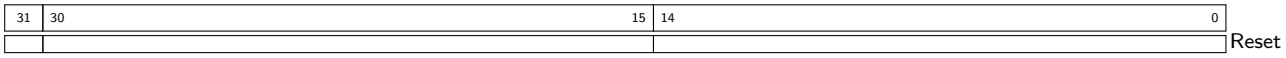
0
Reset





$I2CTIMEOUTVALUE$


31
30
15
14
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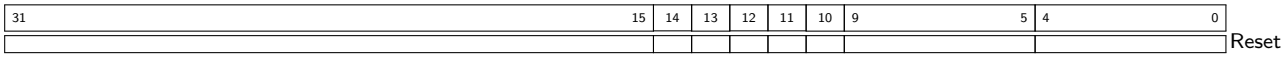
Reset


31
15
14
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12
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5
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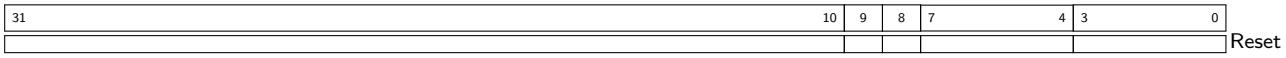
Reset


31
10
9
8
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4
3
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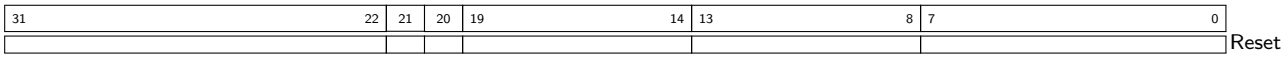
Reset


31
22
21
20
19
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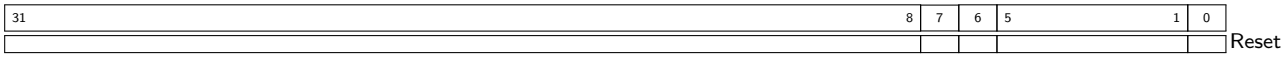
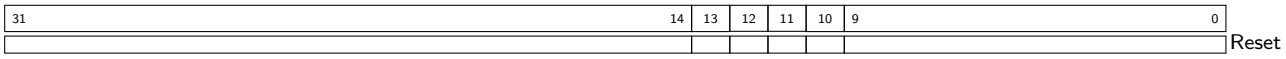
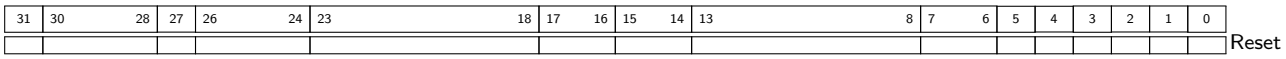
Reset


31
8
7
6
5
1
0
Reset


31
14
13
12
11
10
9
0
Reset


31
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28
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18
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5
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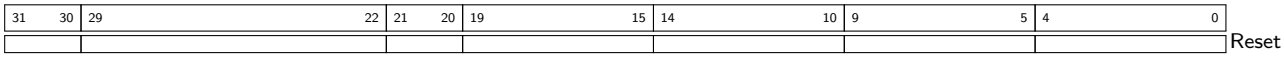
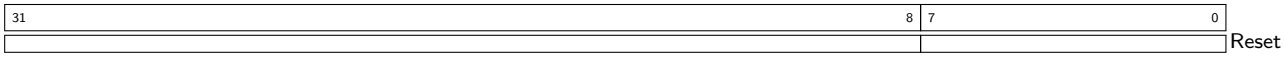
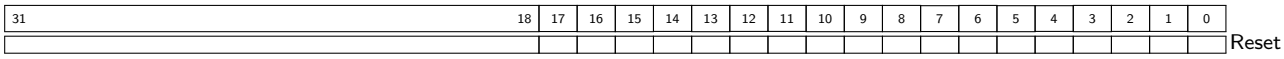
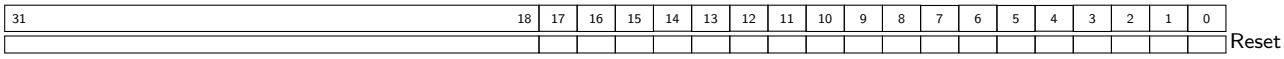
Reset


31 30
29 22
21 20
19 15
14 10
9 5
4 0
Reset


31 8
7 0
Reset


31 18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
Reset


31
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17
16
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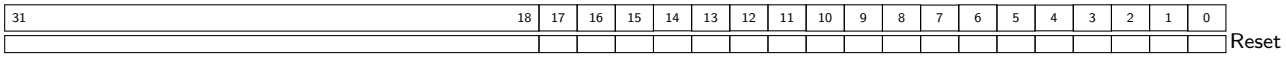
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
Reset


31
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4
3
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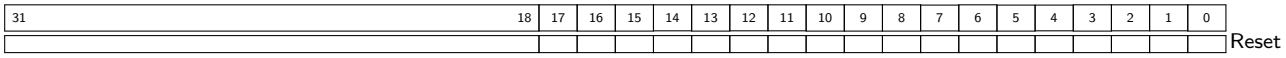
0
Reset


31
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3
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Reset

31	30	14	13	0
				Reset

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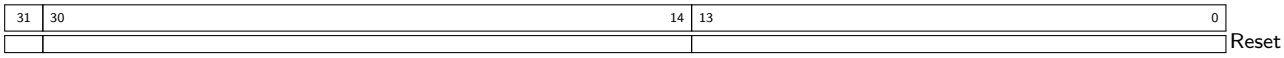
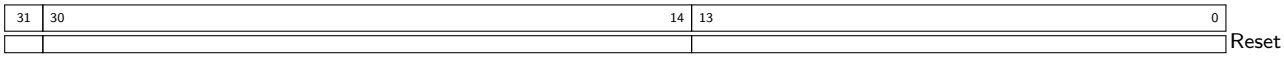
31	30	14	13	0
				Reset

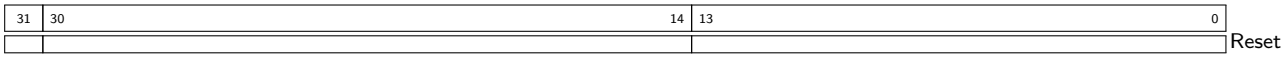
31	30	14	13	0
				Reset

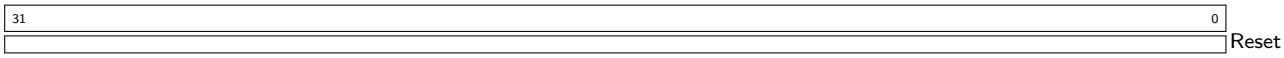
31	30	14	13	0
				Reset

31	30	14	13	0
				Reset


31
30
14
13
0
Reset


31
30
14
13
0
Reset


31
30
14
13
0
Reset


31
0
Reset

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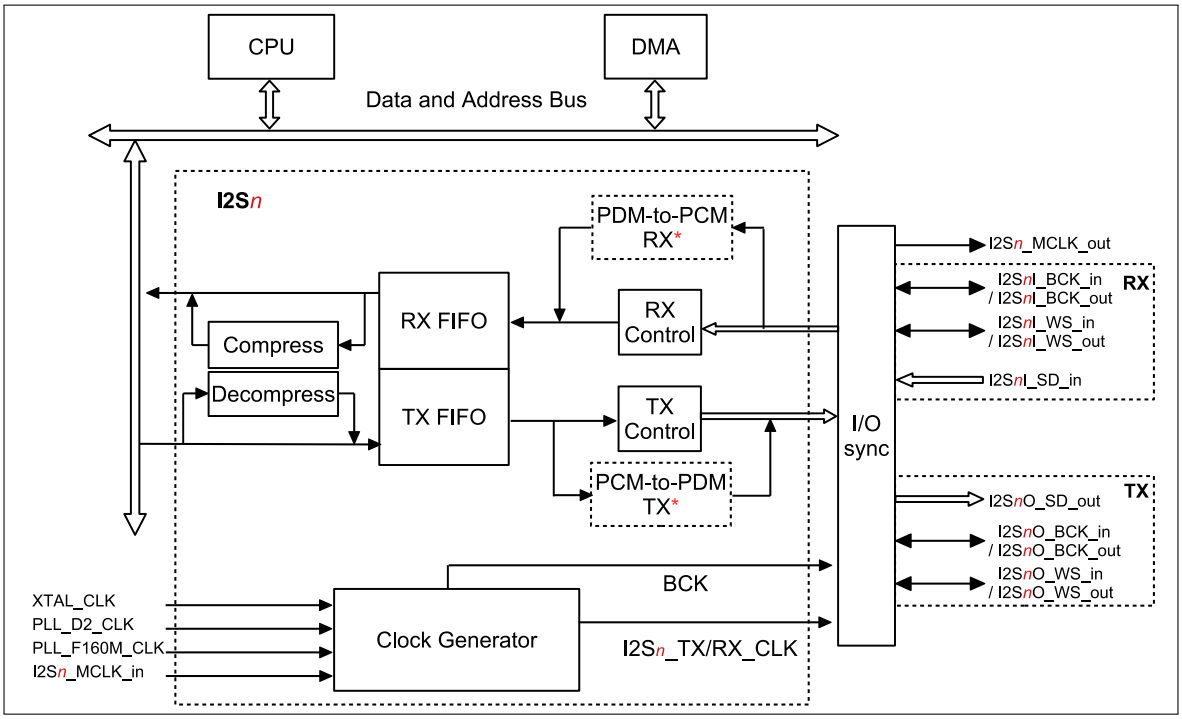
CPU
DMA
Data and Address Bus
I2Sn
PDM-to-PCM RX*
RX FIFO
RX Control
Compress
Decompress
TX FIFO
TX Control
PCM-to-PDM TX*
I/O sync
I2Sn_MCLK_out
I2SnI_BCK_in / I2SnI_BCK_out
I2SnI_WS_in / I2SnI_WS_out
I2SnI_SD_in
RX
I2SnO_SD_out
I2SnO_BCK_in / I2SnO_BCK_out
I2SnO_WS_in / I2SnO_WS_out
TX
BCK
XTAL_CLK
PLL_D2_CLK
PLL_F160M_CLK
I2Sn_MCLK_in
Clock Generator
I2Sn_TX/RX_CLK

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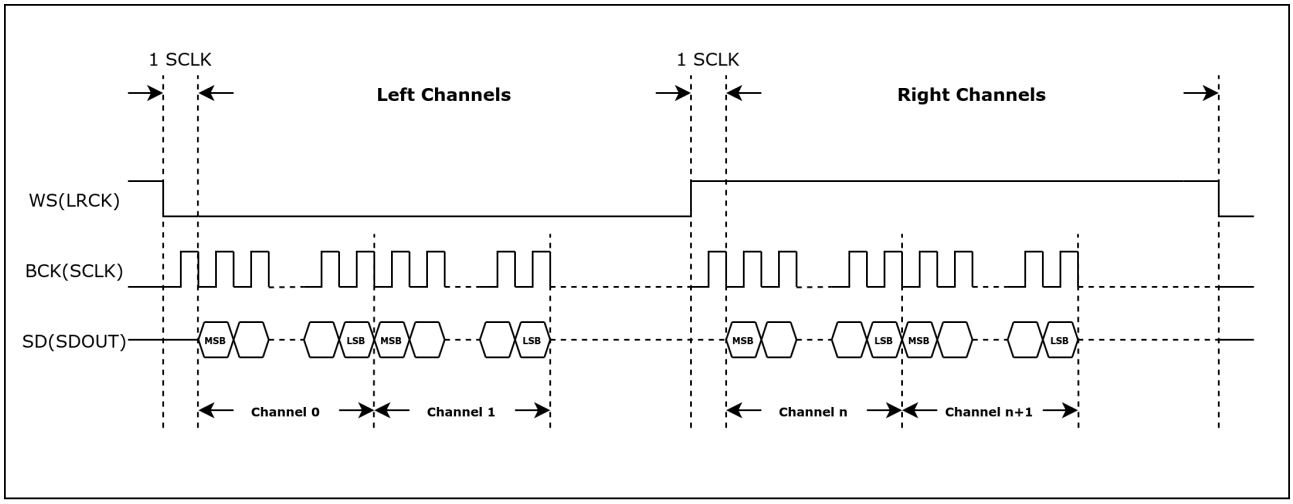
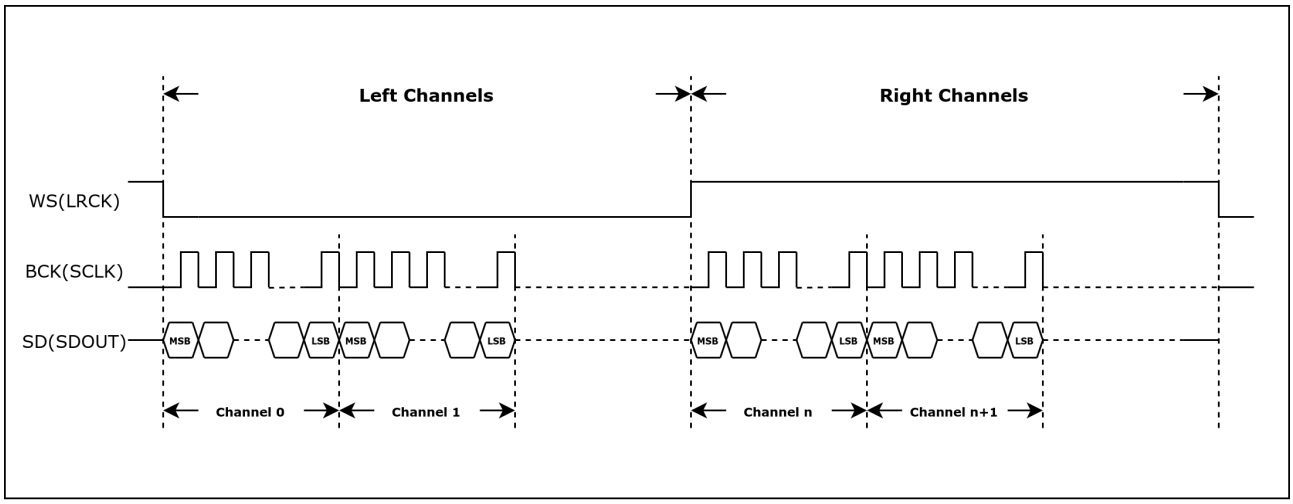
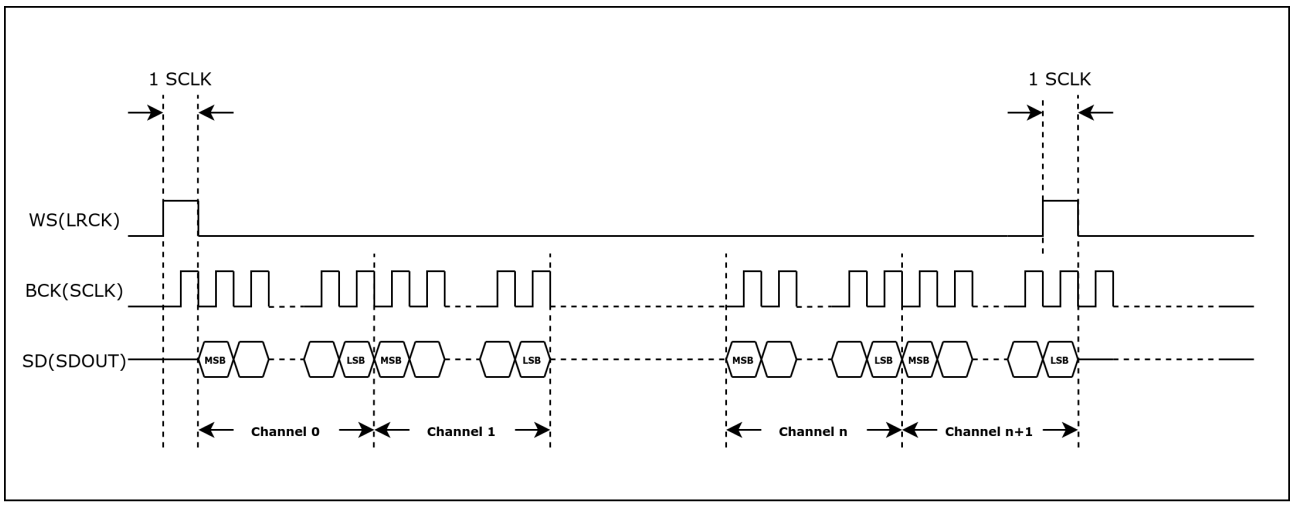
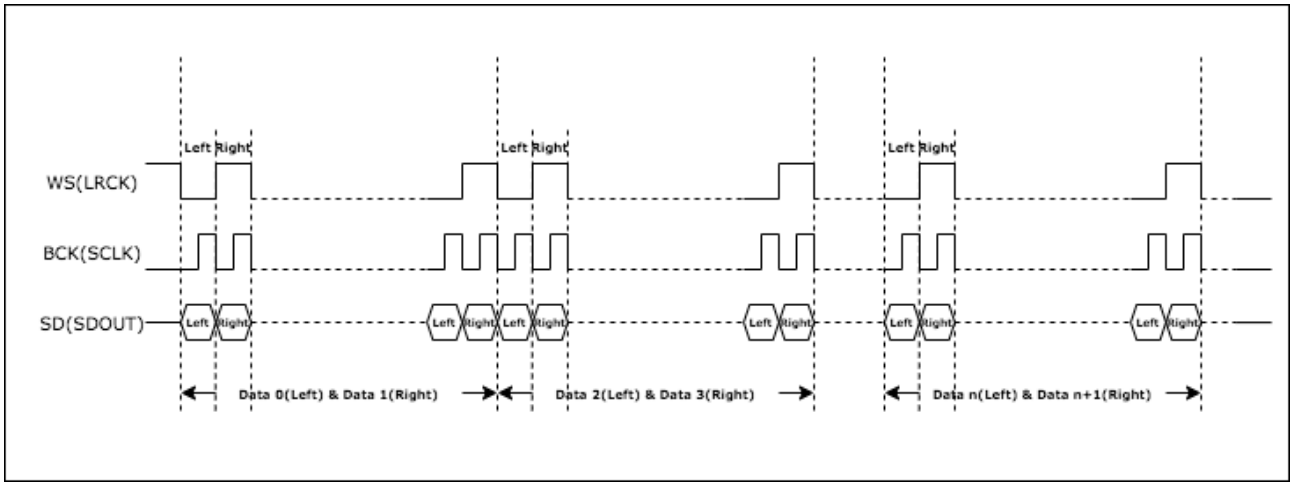

1 SCLK
Left Channels
1 SCLK
Right Channels
WS(LRCK)
BCK(SCLK)
SD(SDOUT)
MSB
LSB
MSB
LSB
MSB
LSB
MSB
LSB
Channel 0
Channel 1
Channel n
Channel n+1


Left Channels
Right Channels
WS(LRCK)
BCK(SCLK)
SD(SDOUT)
MSB
LSB
MSB
LSB
MSB
LSB
MSB
LSB
Channel 0
Channel 1
Channel n
Channel n+1


1 SCLK
1 SCLK
WS(LRCK)
BCK(SCLK)
SD(SDOUT)
MSB
LSB
MSB
LSB
MSB
LSB
MSB
LSB
Channel 0
Channel 1
Channel n
Channel n+1


Left
Right
Left
Right
Left
Right
WS(LRCK)
BCK(SCLK)
SD(SDOUT)
Left
Right
Left
Right
Left
Right
Left
Right
Left
Right
Data 0(Left) & Data 1(Right)
Data 2(Left) & Data 3(Right)
Data n(Left) & Data n+1(Right)

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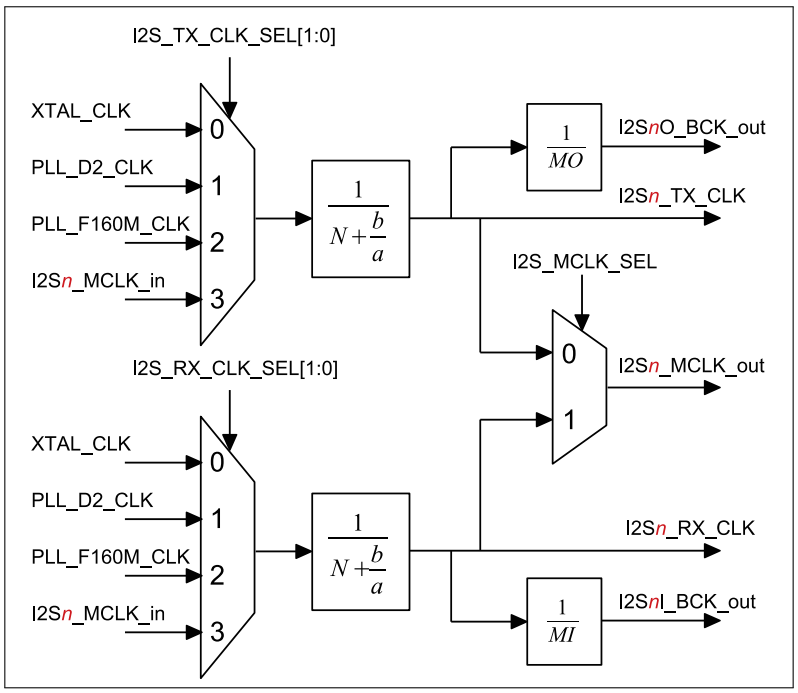
-
-
-



ff

$$f = \frac{f}{+}$$

-
-
-

- $<= \frac{}{2} = 0 = floor([\,]) - 1 = \ =$
- $> \frac{}{2} = 1 = floor([\,]) - 1 = \ =$

$$f = \frac{f}{-}$$

$$= +1$$

$$f = \frac{f}{-}$$

$$= +1$$

-
- ff

-
-

-

-

-

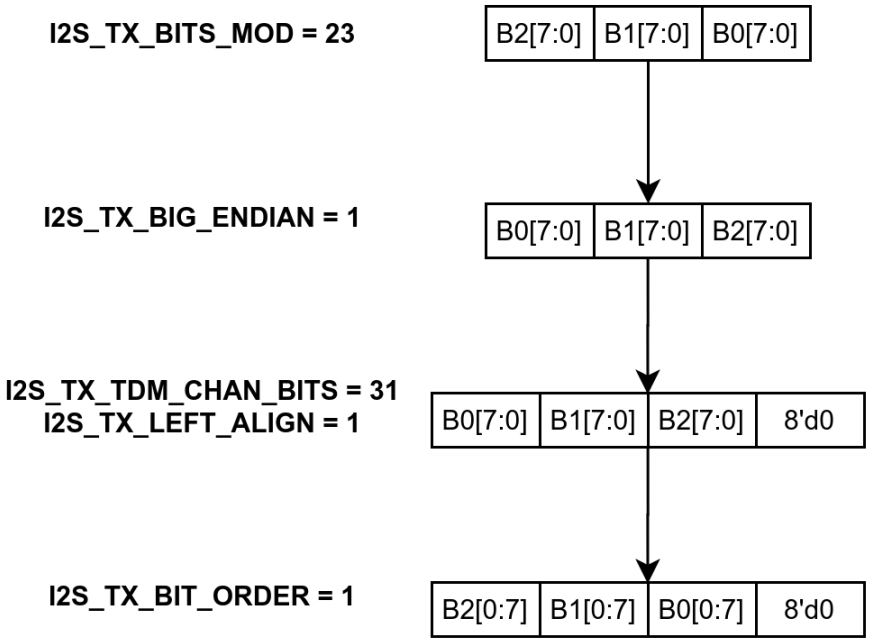
-
-
-
-
-
-

μ

μ

-
-
-
-
- μ
- μ

-
-
-
-


I2S_TX_BITS_MOD = 23
B2[7:0]
B1[7:0]
B0[7:0]
I2S_TX_BIG_ENDIAN = 1
B0[7:0]
B1[7:0]
B2[7:0]
I2S_TX_TDM_CHAN_BITS = 31
I2S_TX_LEFT_ALIGN = 1
B0[7:0]
B1[7:0]
B2[7:0]
8'd0
I2S_TX_BIT_ORDER = 1
B2[0:7]
B1[0:7]
B0[0:7]
8'd0

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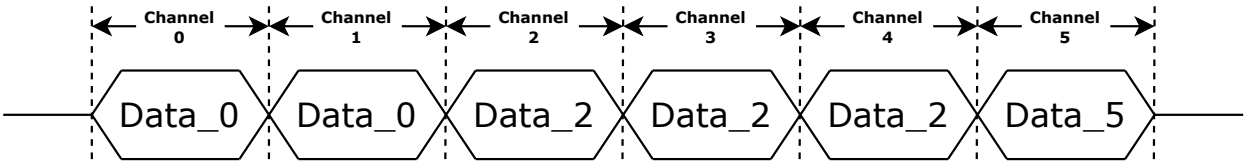
-
-
-



I2S_TX_TDM_CHAN_NUM = 5; I2S_TX_CHAN_EQUAL = 1;
I2S_TX_TDM_CHAN0_EN = 1; I2S_TX_TDM_CHAN1_EN = 0; I2S_TX_TDM_CHAN2_EN = 1;
I2S_TX_TDM_CHAN3_EN = 0; I2S_TX_TDM_CHAN4_EN = 0; I2S_TX_TDM_CHAN5_EN = 1;

-

- f

$$f = \frac{f}{-}$$

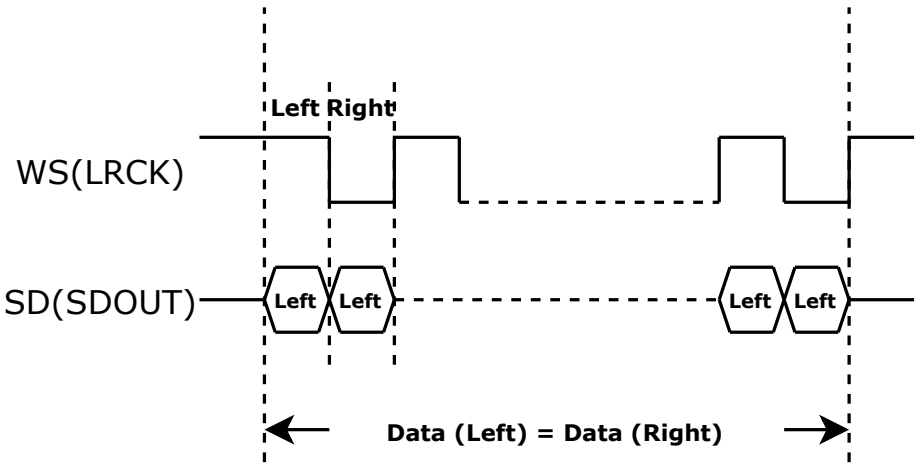
$$= \times$$

f

$$f = \times$$

-

-



I2S_TX_CHAN_MOD = 2; I2S_TX_WS_IDLE_POL = 1;

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-
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-

f

$$f = \frac{f}{-}$$

$$= \times$$

-

-
-
-
-

-

-

μ

μ

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-
-

-
- μ
- μ

    -
    -

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    -

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    -

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    -

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-
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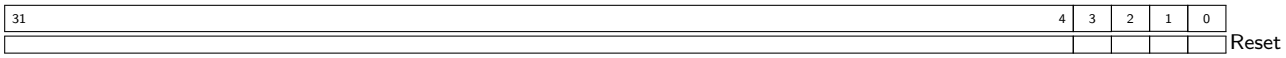
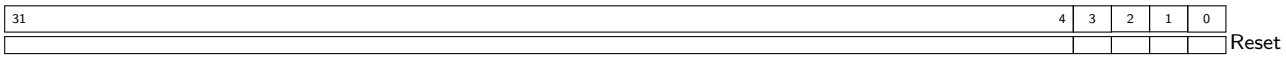
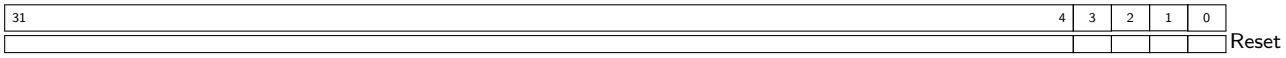
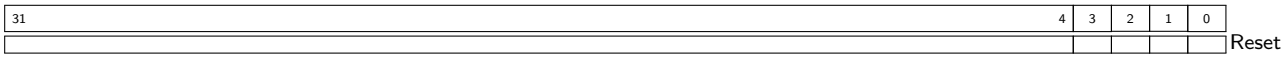

31
4
3
2
1
0
Reset


31
4
3
2
1
0
Reset


31
4
3
2
1
0
Reset


31
4
3
2
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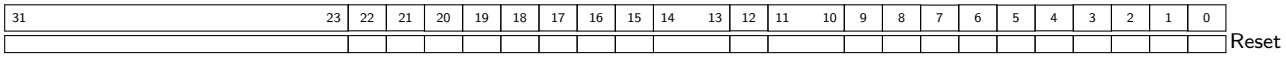
0
Reset



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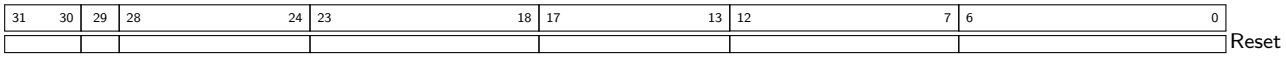
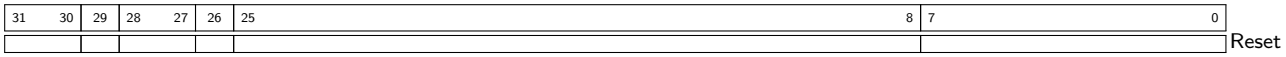
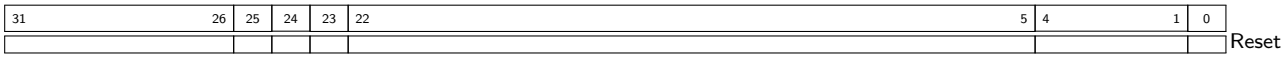
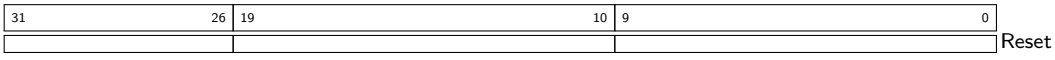
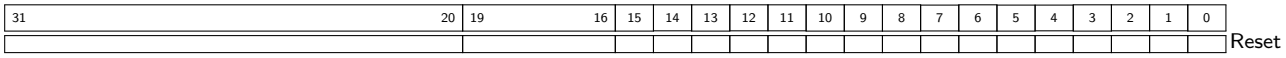

31 30
29
28 24
23 18
17 13
12 7
6 0
Reset


31 30
29
28 27
26
25 8
7 0
Reset


31 26
25
24
23
22 5
4 1
0
Reset


31 26
19 10
9 0
Reset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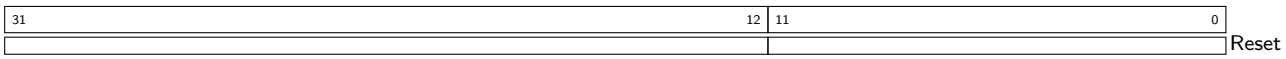
Reset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12
11
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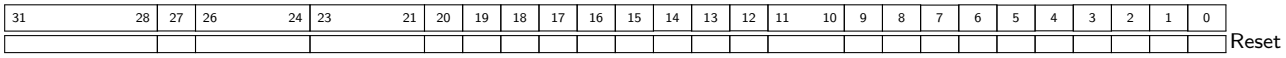
Reset


31 28
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26 24
23 21
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11 10
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Reset

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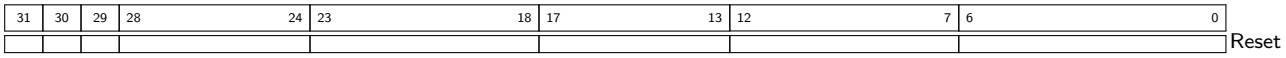
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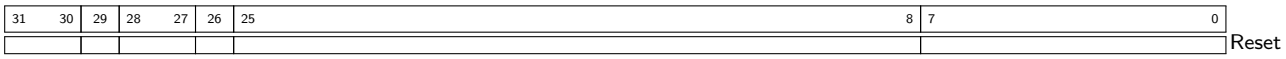
Reset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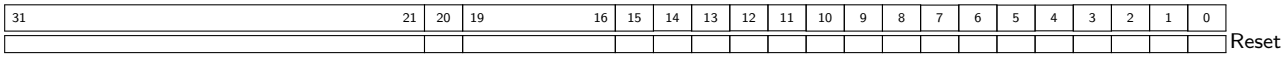
Reset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16
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8
7
6
5
4
3
2
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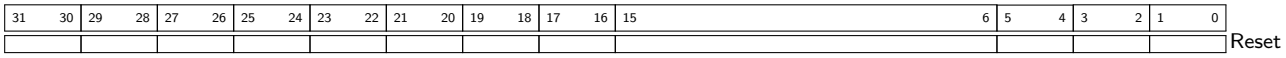
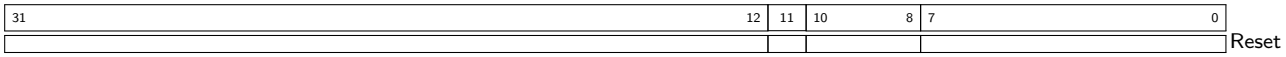
0
Reset

31 28	27	26 18	17 9	8 0	
					Reset

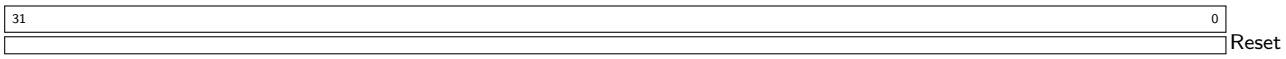
31 30	29 28	27 26	25 24	23 22	21 20	19 18	17 16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0	
																Reset

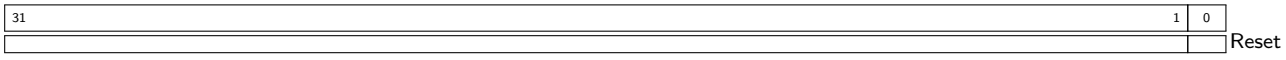
31 28	27	26 18	17 9	8 0	
					Reset

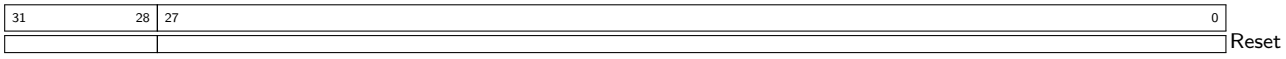




I2SLCFIFOTIMEOUTSHIFT







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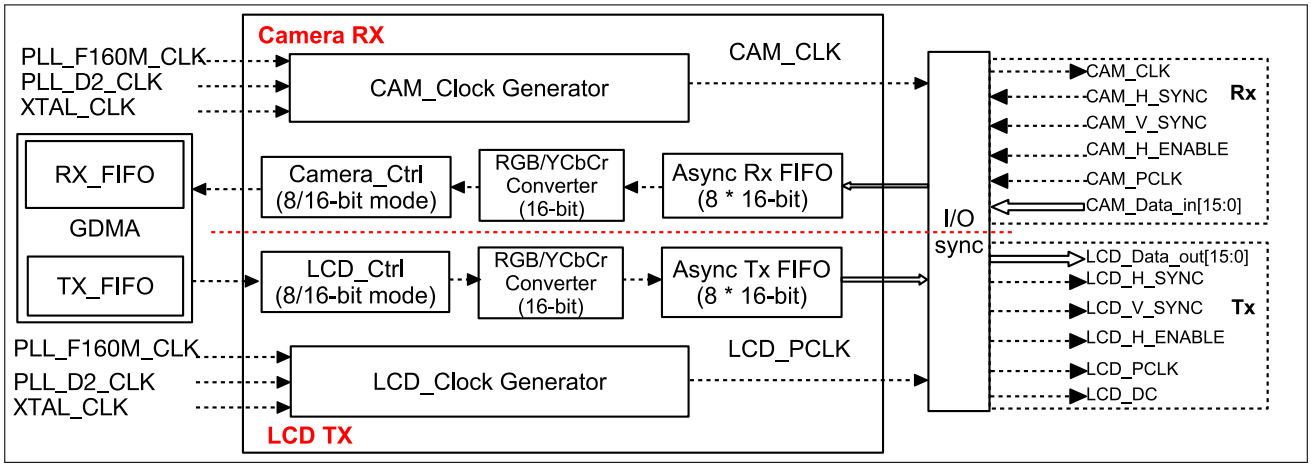
Camera RX
PLL_F160M_CLK
PLL_D2_CLK
XTAL_CLK
CAM_Clock Generator
CAM_CLK
RX_FIFO
GDMA
TX_FIFO
Camera_Ctrl
(8/16-bit mode)
RGB/YCbCr
Converter
(16-bit)
Async Rx FIFO
(8 * 16-bit)
LCD_Ctrl
(8/16-bit mode)
RGB/YCbCr
Converter
(16-bit)
Async Tx FIFO
(8 * 16-bit)
I/O
sync
CAM_CLK
CAM_H_SYNC
CAM_V_SYNC
CAM_H_ENABLE
CAM_PCLK
CAM_Data_in[15:0]
Rx
LCD_Data_out[15:0]
LCD_H_SYNC
LCD_V_SYNC
LCD_H_ENABLE
LCD_PCLK
LCD_DC
Tx
PLL_F160M_CLK
PLL_D2_CLK
XTAL_CLK
LCD_Clock Generator
LCD_PCLK
LCD TX

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-

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-
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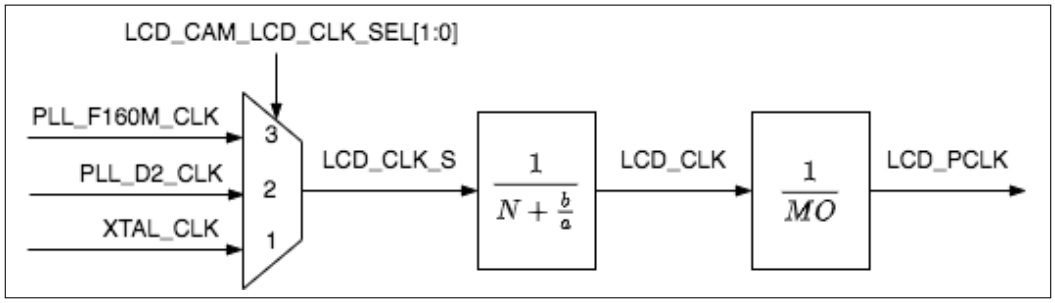
-



ff

$$f = \frac{f}{+}$$

-
-
-

ff

$$f = \frac{f}{-}$$

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-

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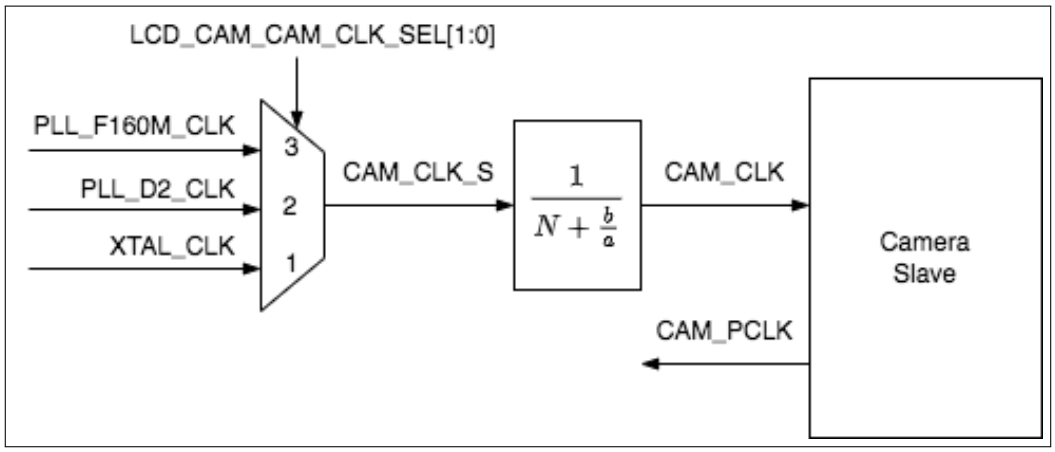
LCD_CAM_CAM_CLK_SEL[1:0]
PLL_F160M_CLK
PLL_D2_CLK
XTAL_CLK
3
2
1
CAM_CLK_S
$\frac{1}{N+\frac{b}{a}}$
CAM_CLK
CAM_PCLK
Camera
Slave

ff

$$f = \frac{f}{+}$$

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-

$Y_iU_iV_i$

-

Y_1	U_1	Y_2	V_2	Y_3	U_3	Y_4	V_4	Y_5	U_5	Y_6	V_6	Y_7	U_7	Y_8	V_8

-

Y_1	U_1	Y_2	Y_3	U_3	Y_4	Y_5	V_5	Y_6	Y_7	V_7	Y_8

-

Y_1	U_1	Y_2	Y_3	V_3	Y_4	Y_5	U_5	Y_6	Y_7	V_7	Y_8

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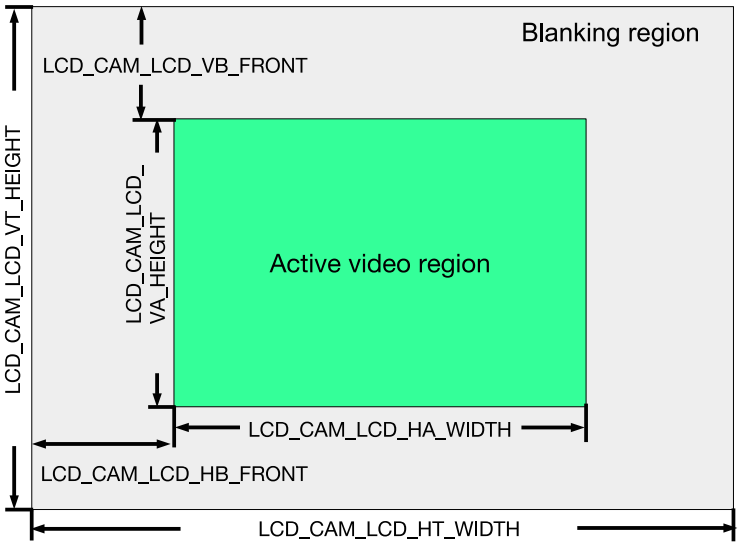
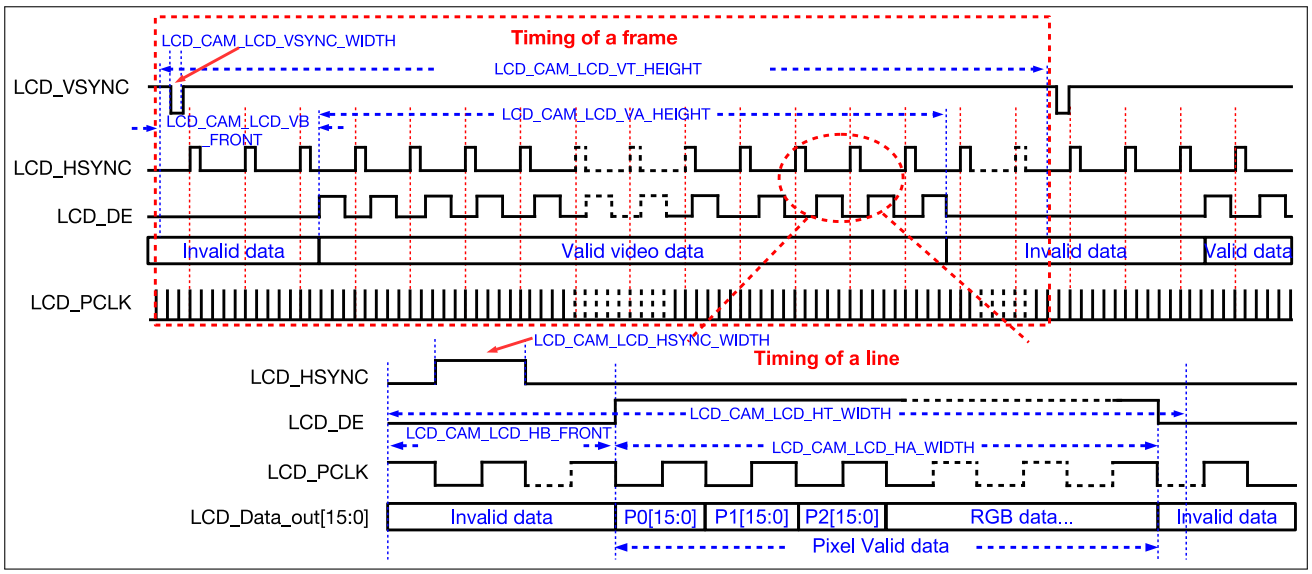

Blanking region
LCD_CAM_LCD_VB_FRONT
LCD_CAM_LCD_VT_HEIGHT
LCD_CAM_LCD_
VA_HEIGHT
Active video region
LCD_CAM_LCD_HA_WIDTH
LCD_CAM_LCD_HB_FRONT
LCD_CAM_LCD_HT_WIDTH


Timing of a frame
LCD_CAM_LCD_VSYNC_WIDTH
LCD_CAM_LCD_VT_HEIGHT
LCD_CAM_LCD_VB_FRONT
LCD_CAM_LCD_VA_HEIGHT
LCD_VSYNC
LCD_HSYNC
LCD_DE
LCD_PCLK
Invalid data
Valid video data
Invalid data
Valid data
LCD_CAM_LCD_HSYNC_WIDTH
Timing of a line
LCD_HSYNC
LCD_DE
LCD_CAM_LCD_HT_WIDTH
LCD_CAM_LCD_HB_FRONT
LCD_CAM_LCD_HA_WIDTH
LCD_PCLK
LCD_Data_out[15:0]
Invalid data
P0[15:0]
P1[15:0]
P2[15:0]
RGB data...
Invalid data
Pixel Valid data

-
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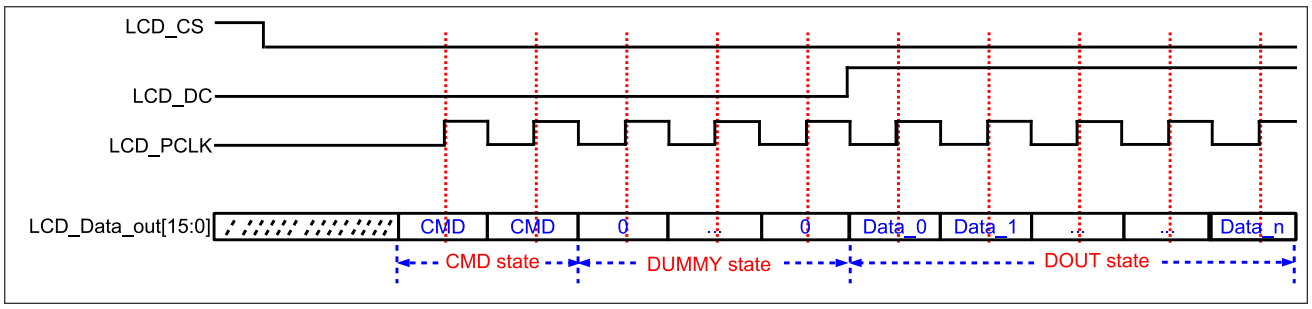
-
-


LCD_CS
LCD_DC
LCD_PCLK
LCD_Data_out[15:0]
CMD
CMD
0
...
0
Data_0
Data_1
...
...
Data_n
CMD state
DUMMY state
DOUT state

- a
- b

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-

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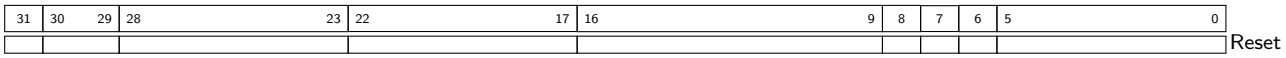
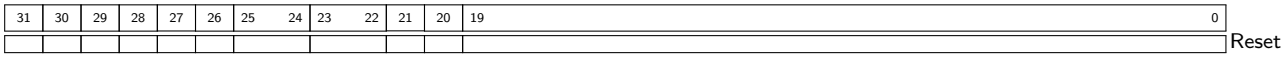
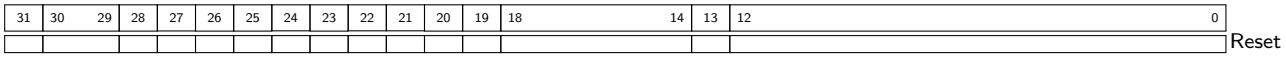
-
-
-



$LCDPCLK\,LCDCLK$

$LCDPCLK\,LCDCLK\,LCDPCLK\,LCDCLK$

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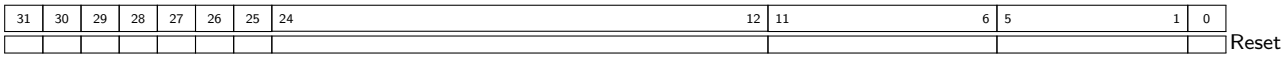
20
19
18
14
13
12
0
Reset


31
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27
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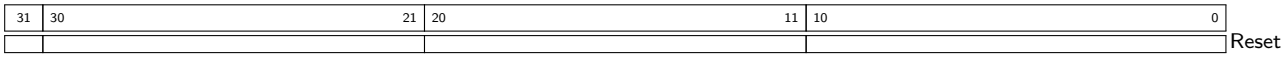
24
12
11
6
5
1
0
Reset


31
30
21
20
11
10
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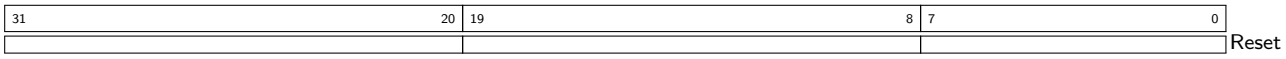
Reset


31
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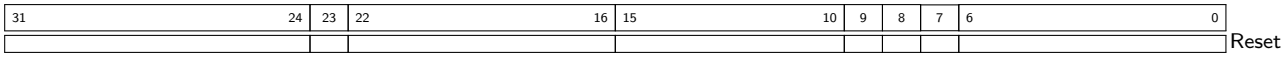
Reset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6
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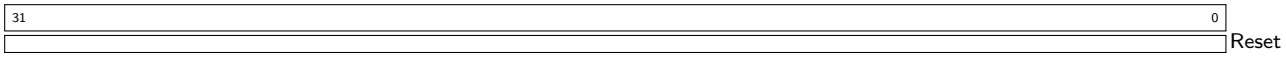
Reset


31
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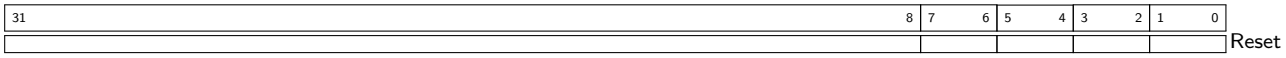
Reset


31
8
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6
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4
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2
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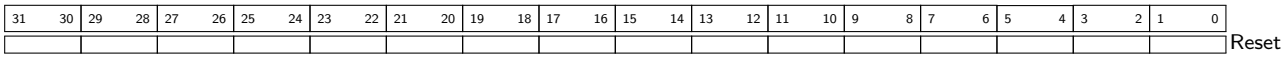
Reset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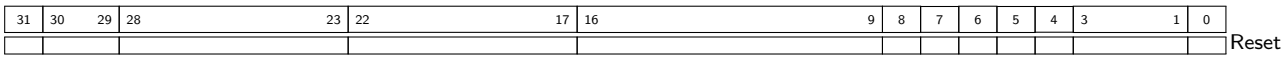
0
Reset


31
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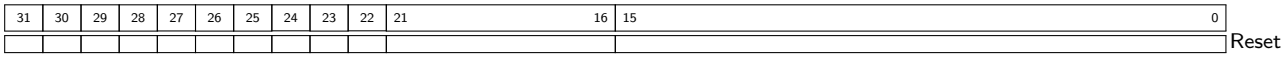
4
3
1
0
Reset


31
30
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26
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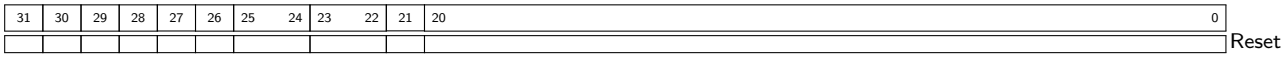
24
23
22
21
16
15
0
Reset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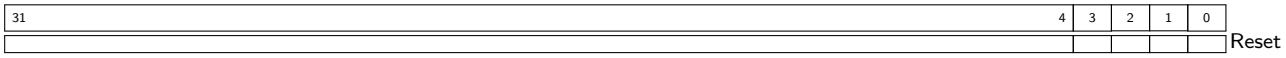
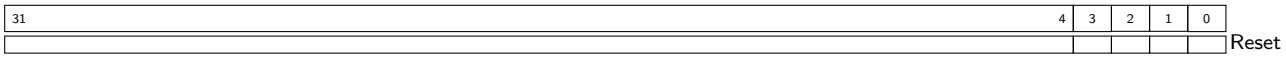
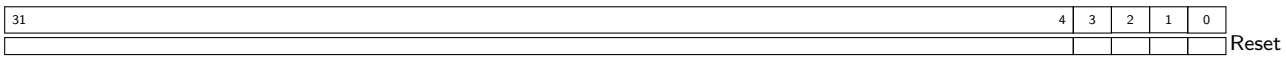
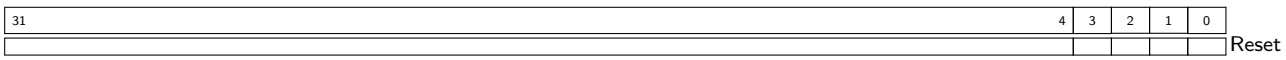
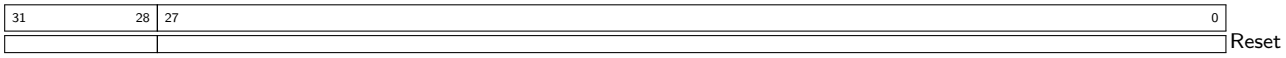
22
21
20
0
Reset


31
4
3
2
1
0
Reset


31
4
3
2
1
0
Reset


31
4
3
2
1
0
Reset


31
4
3
2
1
0
Reset


31
28
27
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Reset

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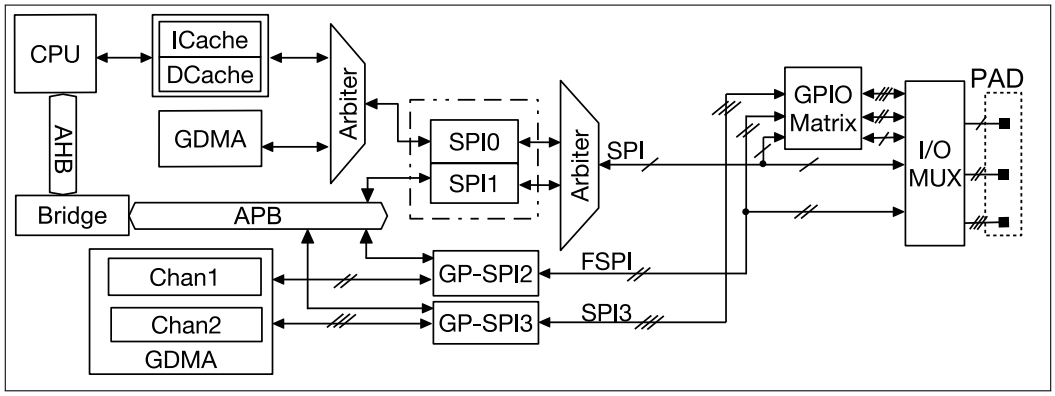
CPU
ICache
DCache
AHB
GDMA
Arbiter
Bridge
APB
SPI0
SPI1
Arbiter
SPI
GPIO
Matrix
I/O
MUX
PAD
Chan1
Chan2
GDMA
GP-SPI2
GP-SPI3
FSPI
SPI3

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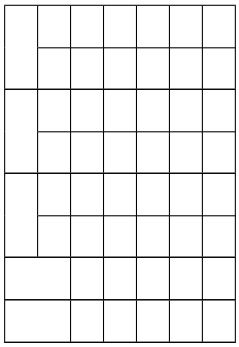

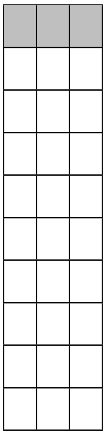

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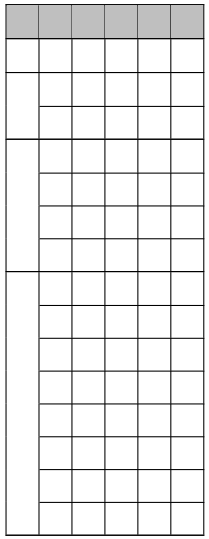

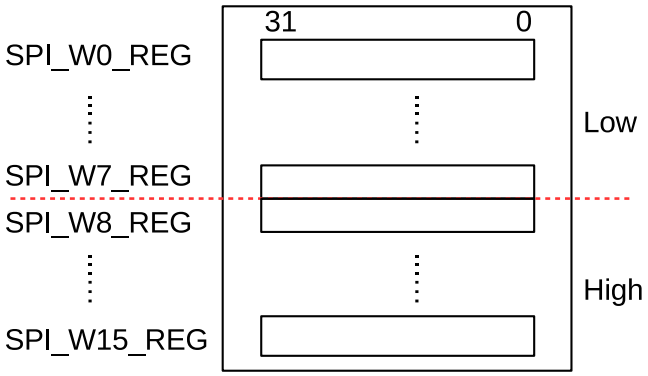
31
0
SPI_W0_REG
SPI_W7_REG
SPI_W8_REG
SPI_W15_REG
Low
High

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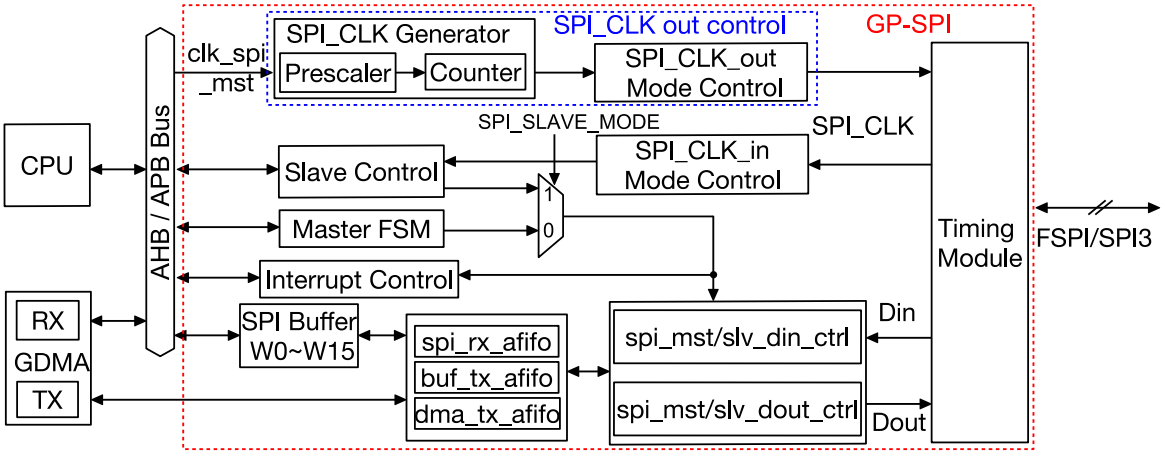
SPI_CLK Generator
Prescaler
Counter
SPI_CLK out control
SPI_CLK_out
Mode Control
GP-SPI
clk_spi
_mst
SPI_SLAVE_MODE
SPI_CLK
SPI_CLK_in
Mode Control
CPU
AHB / APB Bus
Slave Control
Master FSM
Interrupt Control
1
0
Timing
Module
FSPI/SPI3
RX
GDMA
TX
SPI Buffer
W0~W15
spi_rx_afifo
buf_tx_afifo
dma_tx_afifo
spi_mst/slv_din_ctrl
spi_mst/slv_dout_ctrl
Din
Dout

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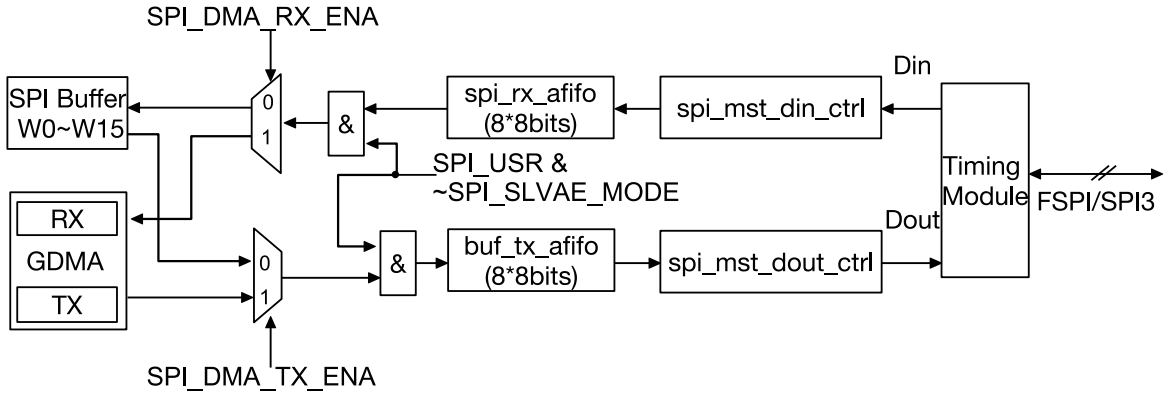
SPI_DMA_RX_ENA
SPI Buffer
W0~W15
0
1
&
spi_rx_afifo
(8*8bits)
spi_mst_din_ctrl
Din
Timing
Module
FSPI/SPI3
SPI_USR &
~SPI_SLVAE_MODE
RX
GDMA
TX
0
1
&
buf_tx_afifo
(8*8bits)
spi_mst_dout_ctrl
Dout
SPI_DMA_TX_ENA

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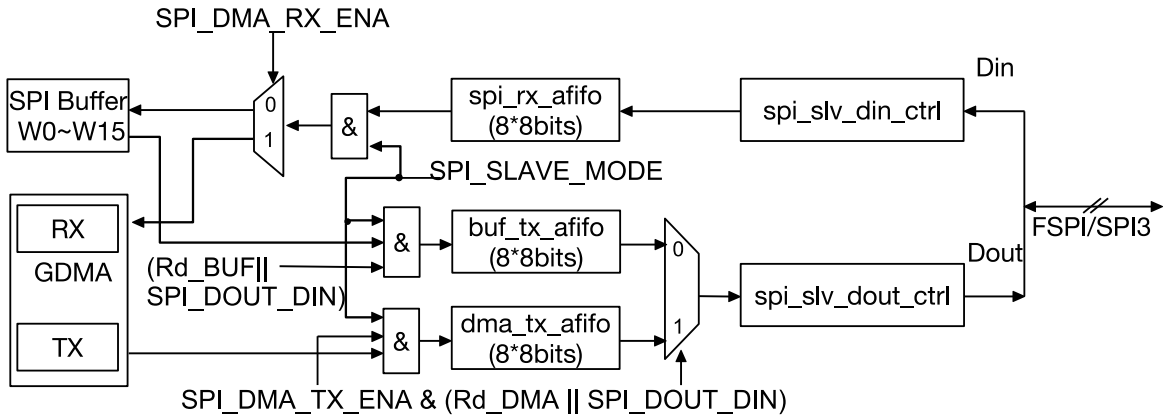
SPI_DMA_RX_ENA
SPI Buffer
W0~W15
0
1
&
spi_rx_afifo
(8*8bits)
spi_slv_din_ctrl
Din
SPI_SLAVE_MODE
RX
GDMA
TX
(Rd_BUF||
SPI_DOUT_DIN)
&
buf_tx_afifo
(8*8bits)
&
dma_tx_afifo
(8*8bits)
0
1
spi_slv_dout_ctrl
Dout
FSPI/SPI3
SPI_DMA_TX_ENA & (Rd_DMA || SPI_DOUT_DIN)

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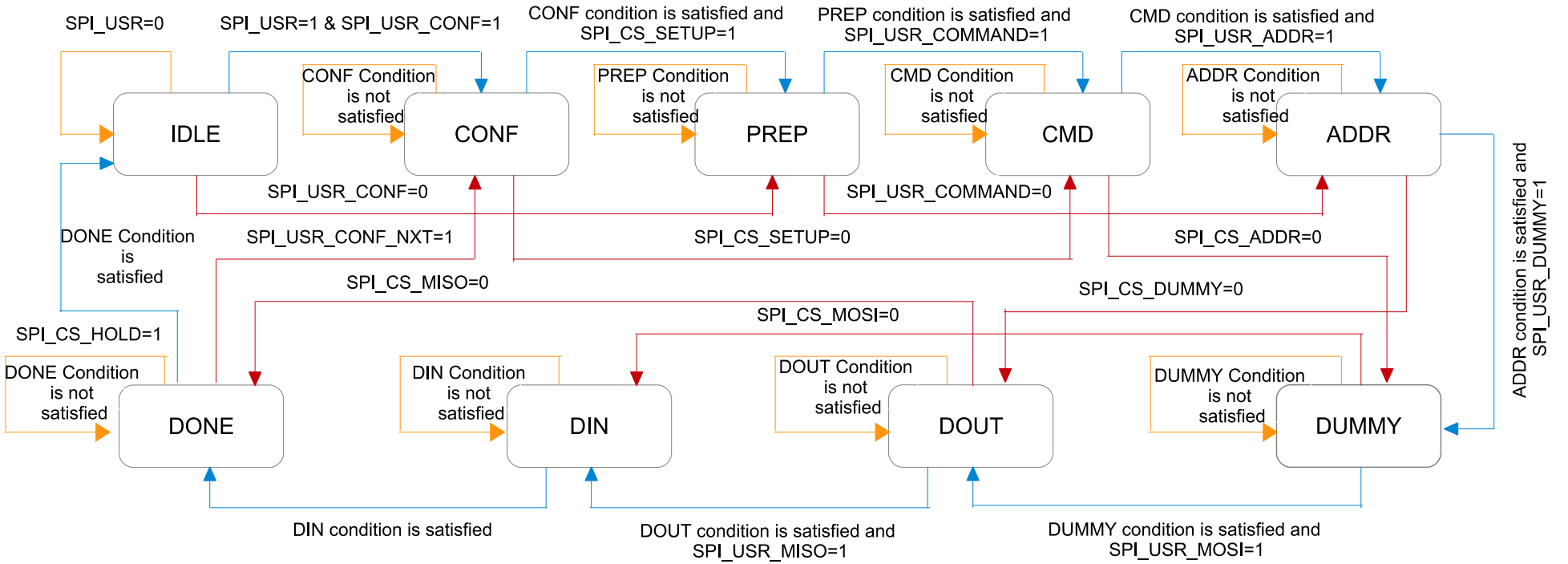
SPI_USR=0
SPI_USR=1 & SPI_USR_CONF=1
CONF condition is satisfied and SPI_CS_SETUP=1
PREP condition is satisfied and SPI_USR_COMMAND=1
CMD condition is satisfied and SPI_USR_ADDR=1
CONF Condition is not satisfied
PREP Condition is not satisfied
CMD Condition is not satisfied
ADDR Condition is not satisfied
IDLE
CONF
PREP
CMD
ADDR
SPI_USR_CONF=0
SPI_USR_COMMAND=0
DONE Condition is satisfied
SPI_USR_CONF_NXT=1
SPI_CS_SETUP=0
SPI_CS_ADDR=0
SPI_CS_MISO=0
SPI_CS_DUMMY=0
SPI_CS_MOSI=0
SPI_CS_HOLD=1
DONE Condition is not satisfied
DIN Condition is not satisfied
DOUT Condition is not satisfied
DUMMY Condition is not satisfied
DONE
DIN
DOUT
DUMMY
ADDR condition is satisfied and SPI_USR_DUMMY=1
DIN condition is satisfied
DOUT condition is satisfied and SPI_USR_MISO=1
DUMMY condition is satisfied and SPI_USR_MOSI=1

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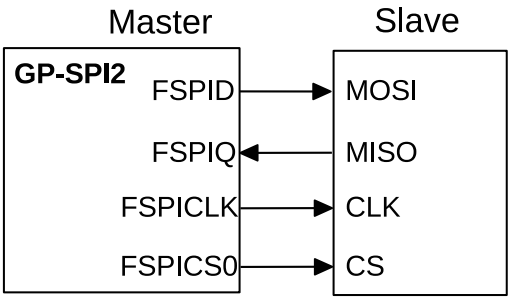
Master
Slave
GP-SPI2
FSPID
FSPIQ
FSPICLK
FSPICS0
MOSI
MISO
CLK
CS

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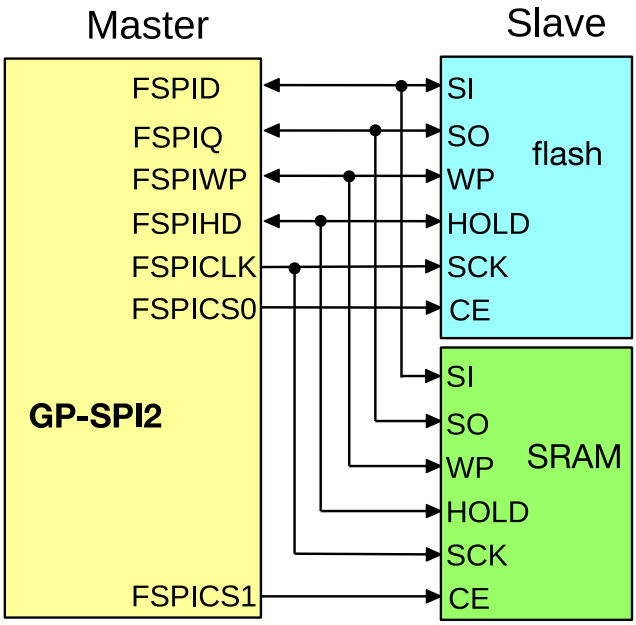
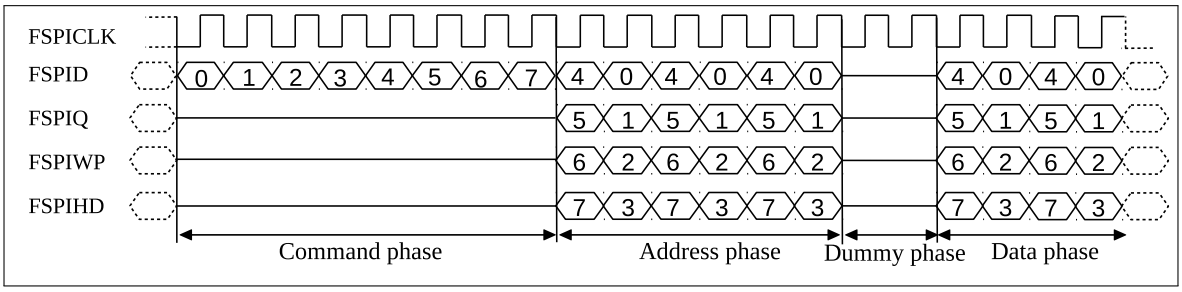

Master
Slave
FSPID
FSPIQ
FSPIWP
FSPIHD
FSPICLK
FSPICS0
GP-SPI2
FSPICS1
SI
SO
WP
HOLD
SCK
CE
flash
SI
SO
WP
HOLD
SCK
CE
SRAM


FSPICLK
FSPID
FSPIQ
FSPIWP
FSPIHD
Command phase
Address phase
Dummy phase
Data phase

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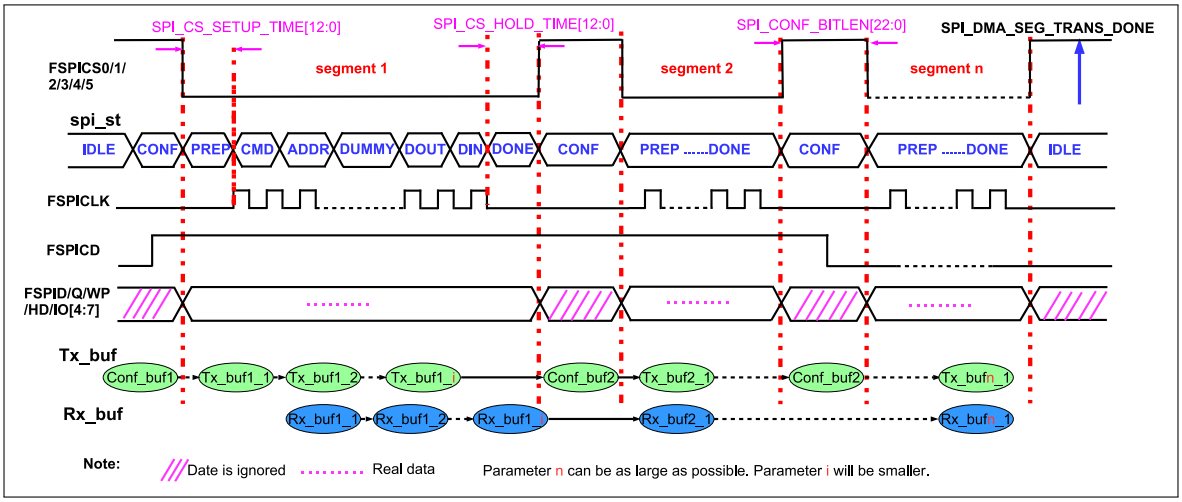
SPI_CS_SETUP_TIME[12:0]
SPI_CS_HOLD_TIME[12:0]
SPI_CONF_BITLEN[22:0]
SPI_DMA_SEG_TRANS_DONE
FSPICS0/1/2/3/4/5
segment 1
segment 2
segment n
spi_st
IDLE
CONF
PREP
CMD
ADDR
DUMMY
DOUT
DIN
DONE
CONF
PREP .....DONE
CONF
PREP .....DONE
IDLE
FSPICLK
FSPICD
FSPID/Q/WP/HD/IO[4:7]
Tx_buf
Conf_buf1
Tx_buf1_1
Tx_buf1_2
Tx_buf1_i
Conf_buf2
Tx_buf2_1
Conf_buf2
Tx_bufn_1
Rx_buf
Rx_buf1_1
Rx_buf1_2
Rx_buf1_i
Rx_buf2_1
Rx_bufn_1
Note:
Date is ignored
Real data
Parameter n can be as large as possible. Parameter i will be smaller.

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$$(SPICONFBITLEN + 5) \times T_{APBCLK}$$

$\mu s f$

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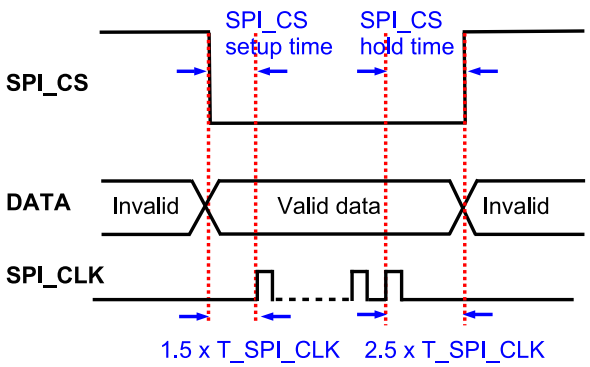
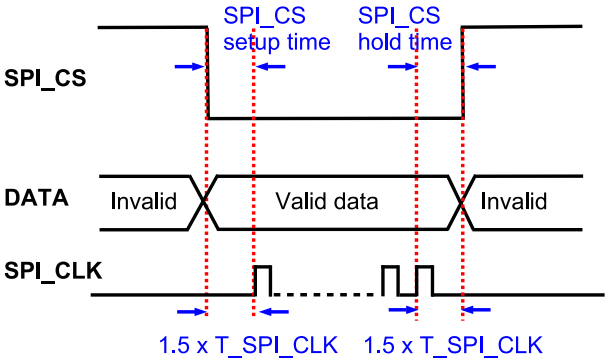


Register Configurations:

SPI_CS_SETUP = 1; SPI_CS_SETUP_TIME = 0;
SPI_CS_HOLD = 1; SPI_CS_HOLD_TIME = 1.



Register Configurations:

SPI_CS_SETUP = 1; SPI_CS_SETUP_TIME = 0;
SPI_CS_HOLD = 1; SPI_CS_HOLD_TIME = 0.

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f

$$f = \frac{f}{}$$

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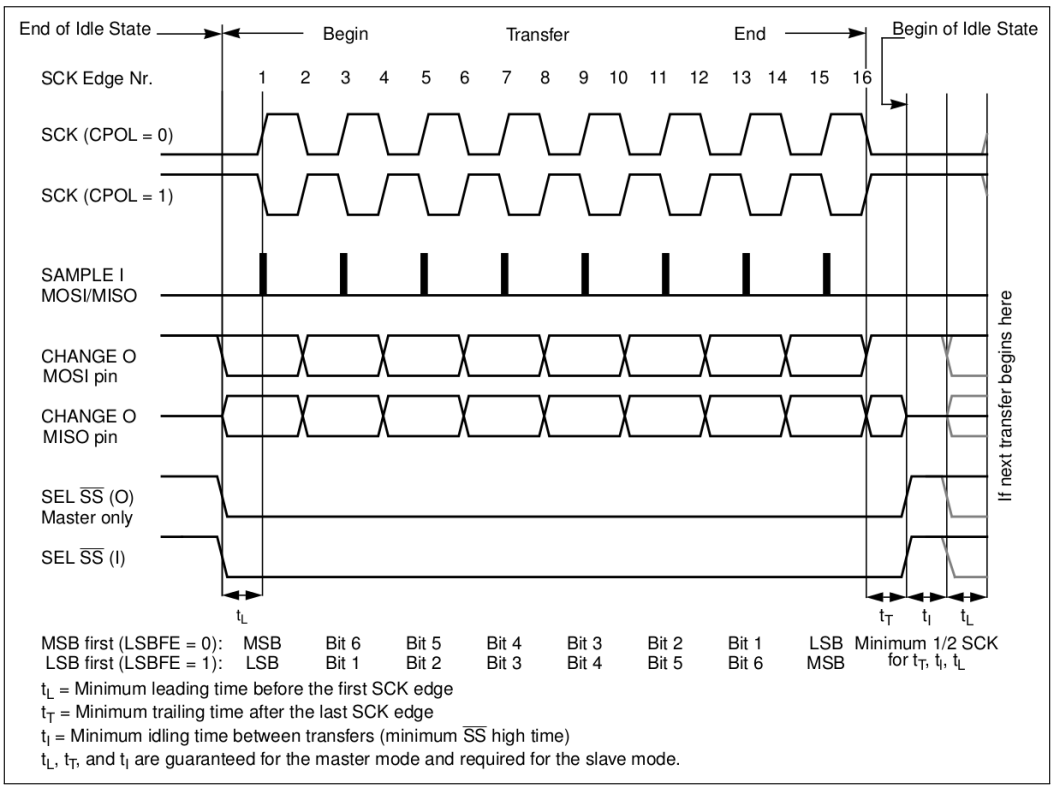
- ff
- fff

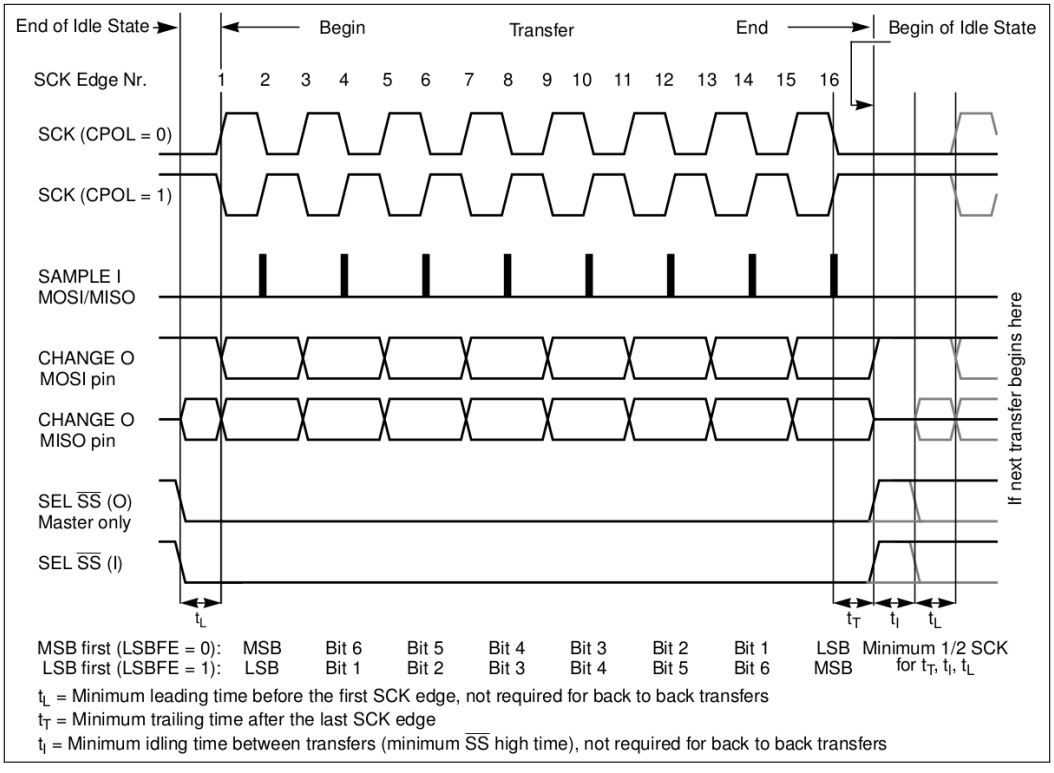


t_L = Minimum leading time before the first SCK edge

t_T = Minimum trailing time after the last SCK edge

t_I = Minimum idling time between transfers (minimum $\overline{SS}$ high time)

t_L, t_T, and t_I are guaranteed for the master mode and required for the slave mode.



t_L = Minimum leading time before the first SCK edge, not required for back to back transfers

t_T = Minimum trailing time after the last SCK edge

t_I = Minimum idling time between transfers (minimum $\overline{SS}$ high time), not required for back to back transfers

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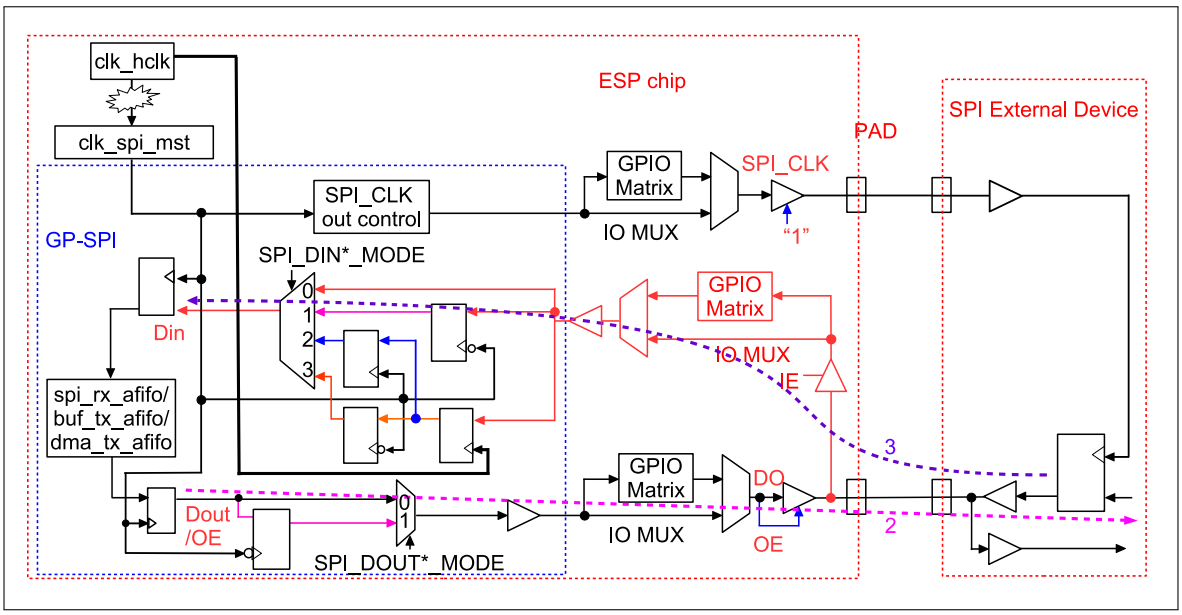
clk_hclk
clk_spi_mst
ESP chip
SPI External Device
PAD
GPIO Matrix
SPI_CLK
IO MUX
"1"
SPI_CLK out control
GP-SPI
SPI_DIN*_MODE
Din
spi_rx_afifo/ buf_tx_afifo/ dma_tx_afifo
Dout /OE
SPI_DOUT*_MODE
DO
OE

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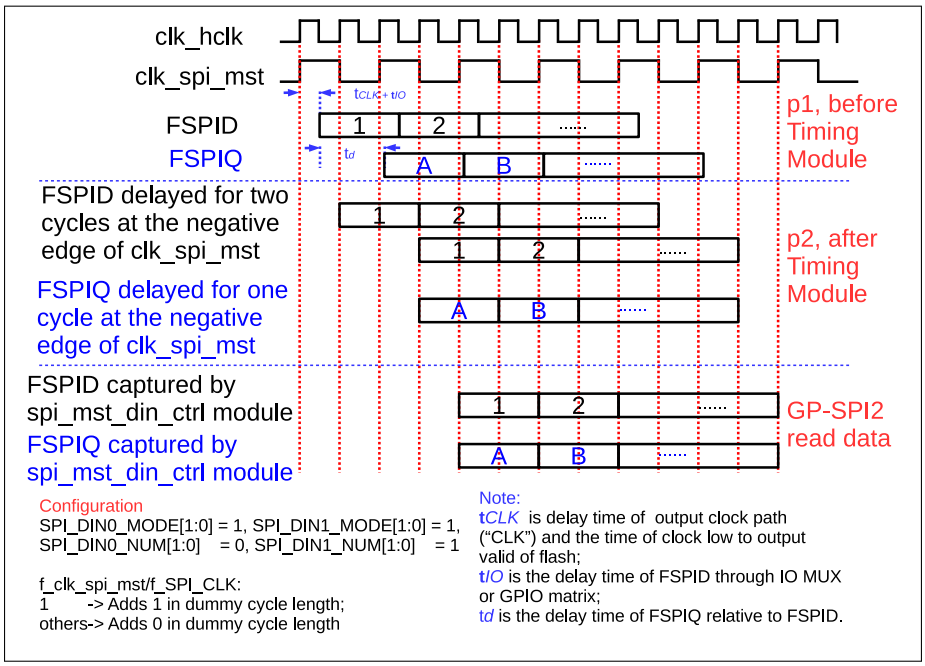
clk_hclk
clk_spi_mst
FSPID
FSPIQ
p1, before Timing Module
FSPID delayed for two cycles at the negative edge of clk_spi_mst
FSPIQ delayed for one cycle at the negative edge of clk_spi_mst
p2, after Timing Module
FSPID captured by spi_mst_din_ctrl module
FSPIQ captured by spi_mst_din_ctrl module
GP-SPI2 read data
Configuration
SPI_DIN0_MODE[1:0] = 1, SPI_DIN1_MODE[1:0] = 1,
SPI_DIN0_NUM[1:0] = 0, SPI_DIN1_NUM[1:0] = 1
f_clk_spi_mst/f_SPI_CLK:
1 -> Adds 1 in dummy cycle length;
others-> Adds 0 in dummy cycle length
Note:
tCLK is delay time of output clock path ("CLK") and the time of clock low to output valid of flash;
tIO is the delay time of FSPID through IO MUX or GPIO matrix;
td is the delay time of FSPIQ relative to FSPID.

$f_{clkspimst} f_{SPICLK}$

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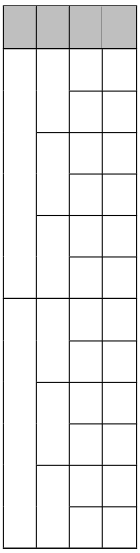

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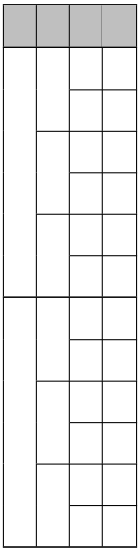

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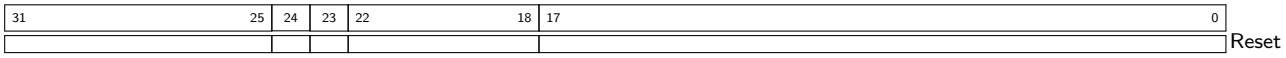
31
25
24
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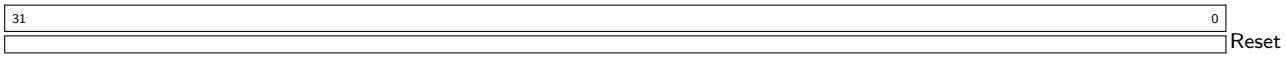
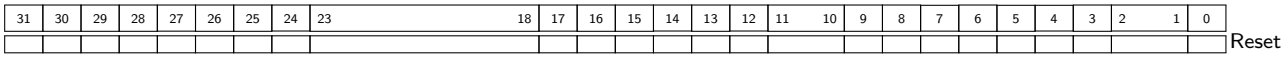
0
Reset


31
0
Reset


31
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1
0
Reset

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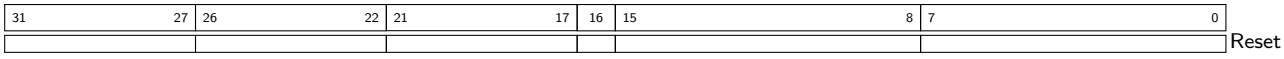
31
27
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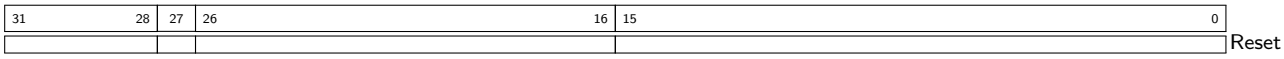
Reset


31
28
27
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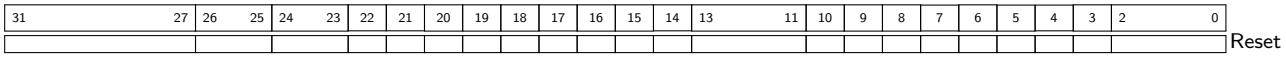
31 27
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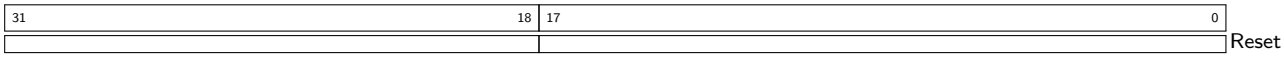
31
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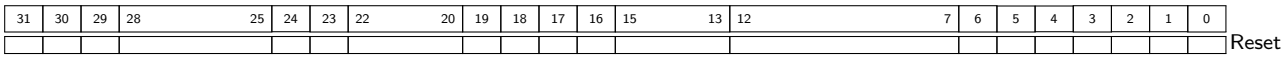
Reset


31
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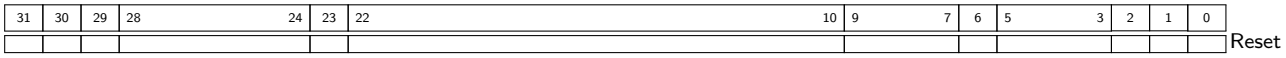
Reset


31
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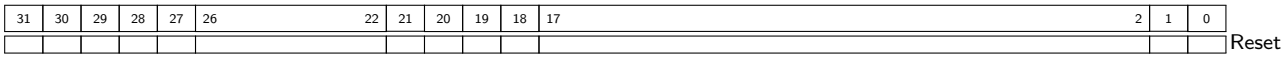
Reset


31
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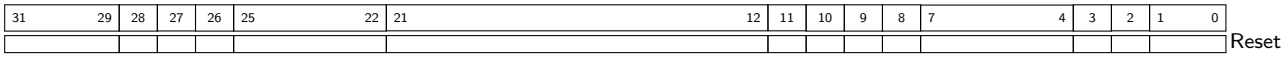
Reset


31 29
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25 22
21 12
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1 0
Reset

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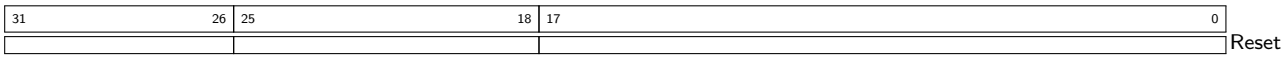
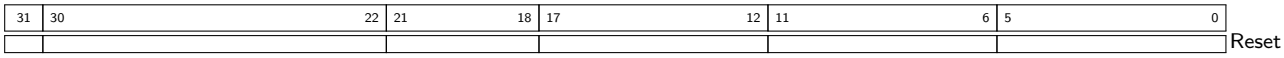
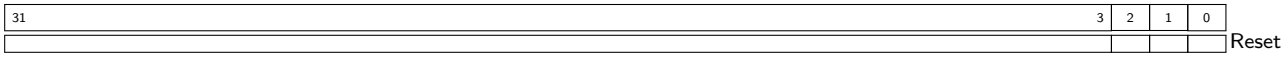

31 26
25 18
17 0
Reset



f



31 17	16	15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0	
										Reset

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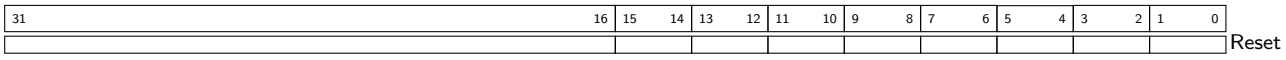
31
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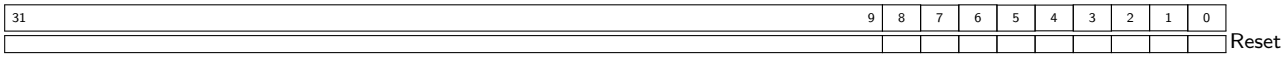
Reset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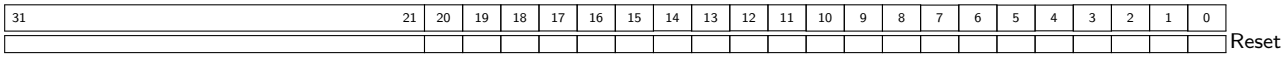
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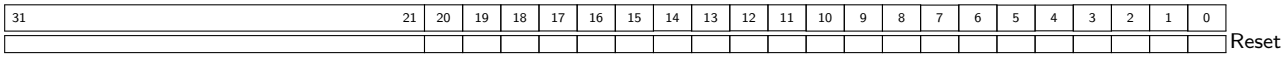
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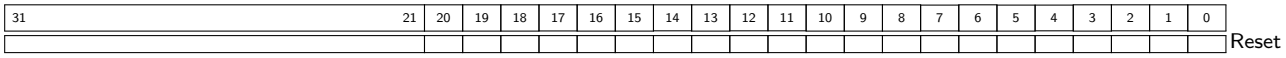
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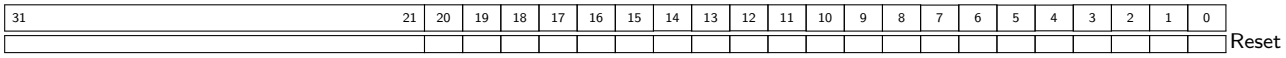
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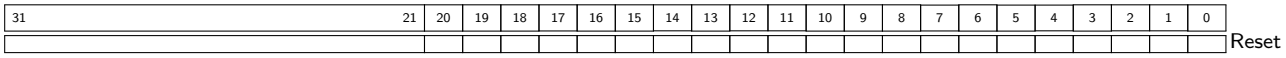
Reset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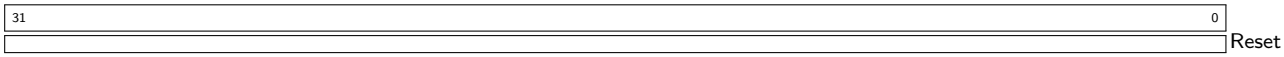
Reset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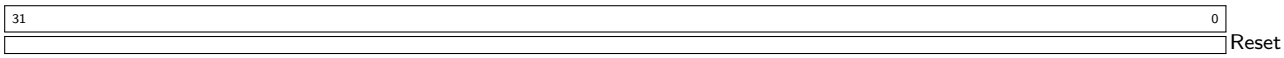
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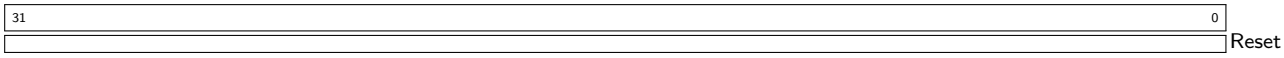
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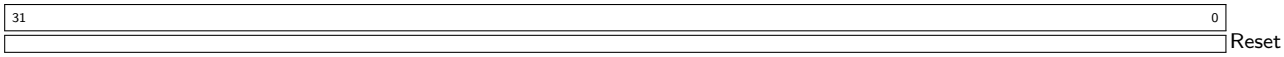
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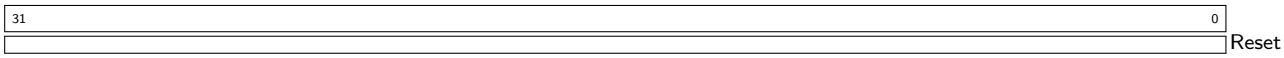
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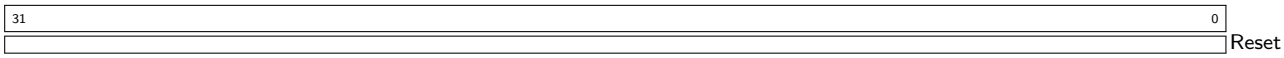
Reset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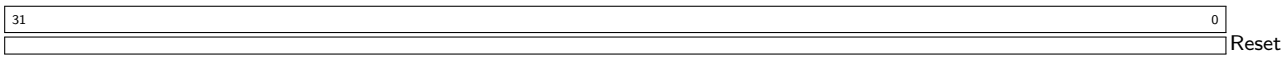
Reset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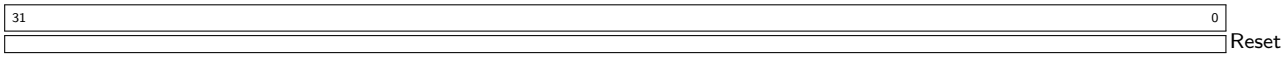
Reset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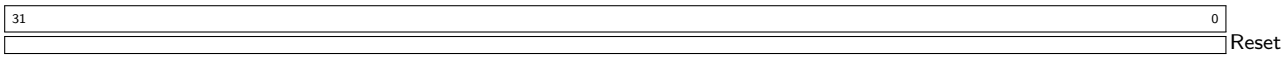
Reset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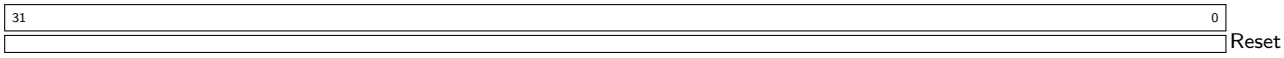
Reset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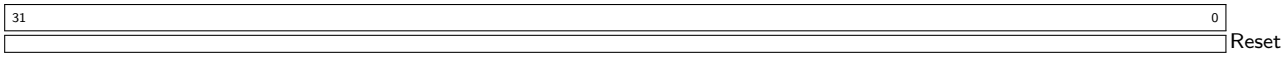
Reset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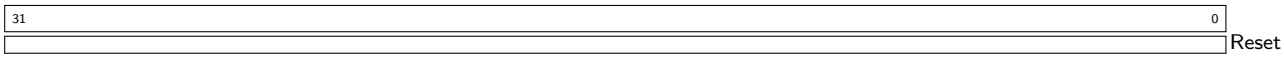
Reset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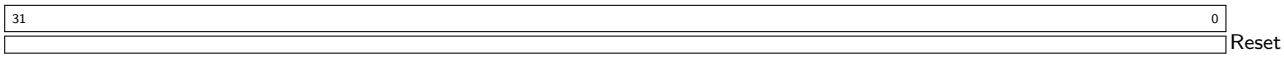
Reset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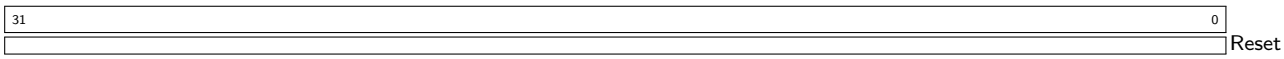
Reset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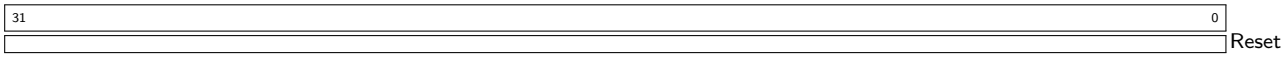
Reset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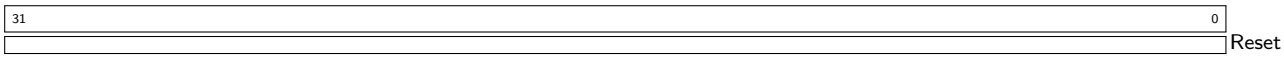
Reset


31
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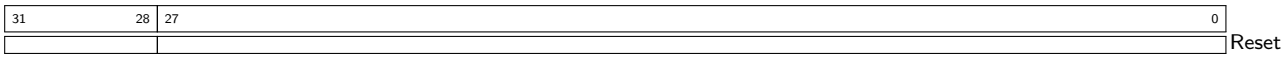
Reset


31
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Reset

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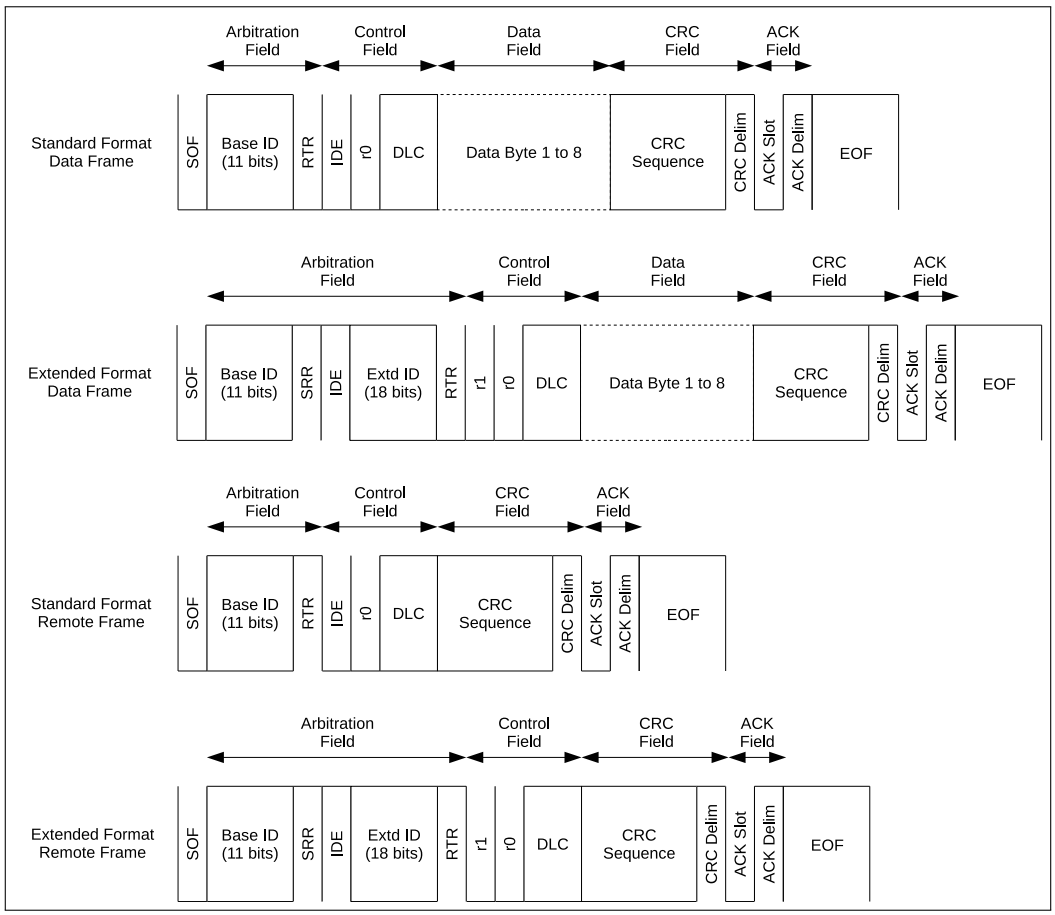
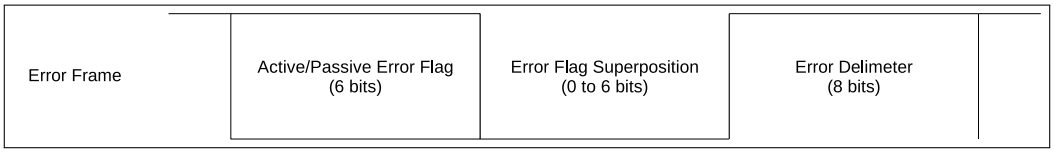
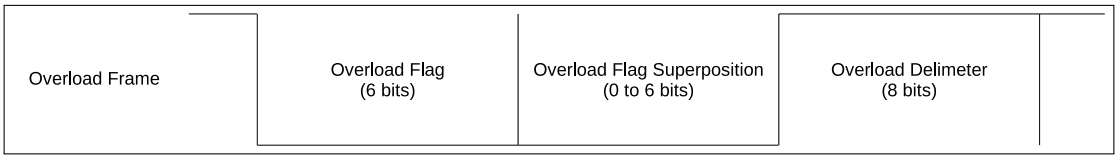

Arbitration Field
Control Field
Data Field
CRC Field
ACK Field
Standard Format Data Frame
SOF
Base ID (11 bits)
RTR
IDE
r0
DLC
Data Byte 1 to 8
CRC Sequence
CRC Delim
ACK Slot
ACK Delim
EOF
Extended Format Data Frame
SRR
Extd ID (18 bits)
RTR
r1
r0
Standard Format Remote Frame
Extended Format Remote Frame

-


Error Frame
Active/Passive Error Flag
(6 bits)
Error Flag Superposition
(0 to 6 bits)
Error Delimeter
(8 bits)


Overload Frame
Overload Flag
(6 bits)
Overload Flag Superposition
(0 to 6 bits)
Overload Delimeter
(8 bits)

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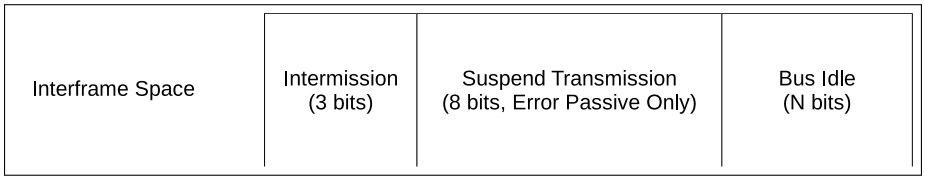
Interframe Space
Intermission
(3 bits)
Suspend Transmission
(8 bits, Error Passive Only)
Bus Idle
(N bits)

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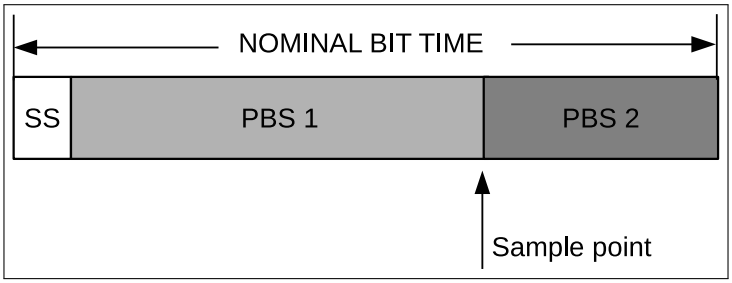
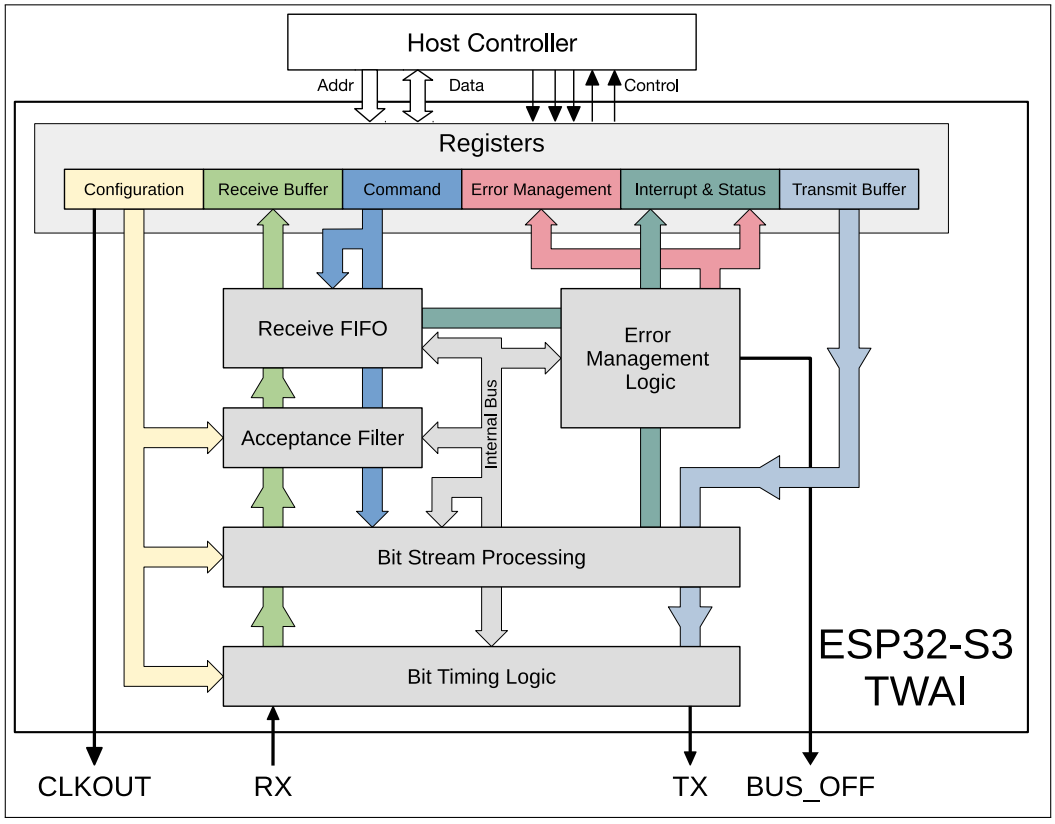

NOMINAL BIT TIME
SS
PBS 1
PBS 2
Sample point


Host Controller
Addr
Data
Control
Registers
Configuration
Receive Buffer
Command
Error Management
Interrupt & Status
Transmit Buffer
Receive FIFO
Error Management Logic
Acceptance Filter
Internal Bus
Bit Stream Processing
Bit Timing Logic
ESP32-S3 TWAI
CLKOUT
RX
TX
BUS_OFF

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-

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-
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- $TqCLK$
  $TqCLK^{121110}$
-

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	1	2	3	3	4	4	4	4

				1	2	2	2	2

						1	2	2

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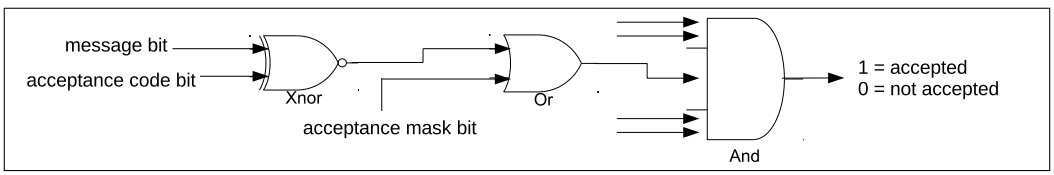
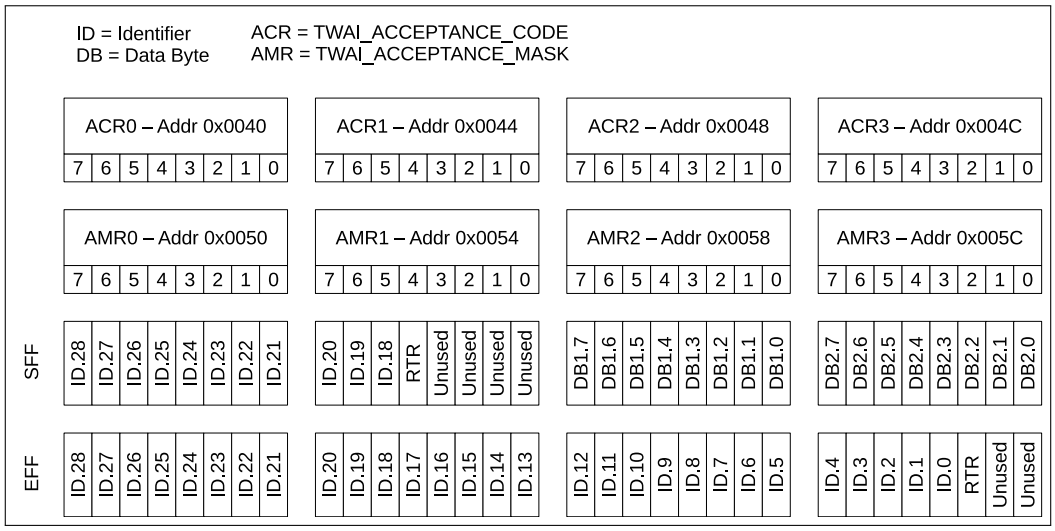
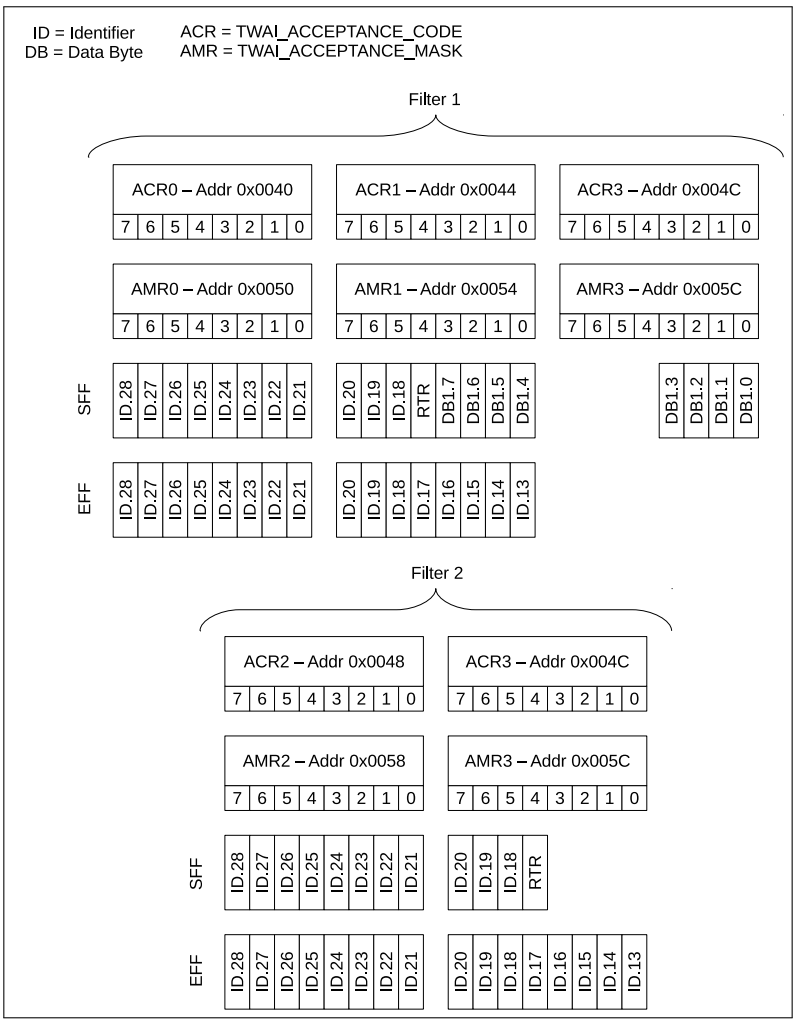
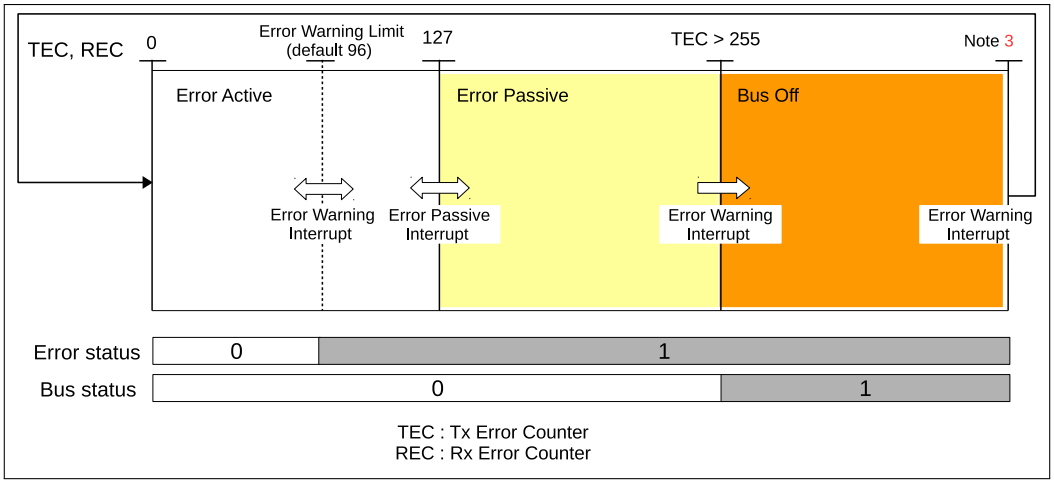

message bit
acceptance code bit
Xnor
acceptance mask bit
Or
And
1 = accepted
0 = not accepted


ID = Identifier
DB = Data Byte
ACR = TWAI_ACCEPTANCE_CODE
AMR = TWAI_ACCEPTANCE_MASK
ACR0 – Addr 0x0040
ACR1 – Addr 0x0044
ACR2 – Addr 0x0048
ACR3 – Addr 0x004C
AMR0 – Addr 0x0050
AMR1 – Addr 0x0054
AMR2 – Addr 0x0058
AMR3 – Addr 0x005C
7 6 5 4 3 2 1 0
SFF
ID.28 ID.27 ID.26 ID.25 ID.24 ID.23 ID.22 ID.21
ID.20 ID.19 ID.18 RTR Unused Unused Unused Unused
DB1.7 DB1.6 DB1.5 DB1.4 DB1.3 DB1.2 DB1.1 DB1.0
DB2.7 DB2.6 DB2.5 DB2.4 DB2.3 DB2.2 DB2.1 DB2.0
EFF
ID.28 ID.27 ID.26 ID.25 ID.24 ID.23 ID.22 ID.21
ID.20 ID.19 ID.18 ID.17 ID.16 ID.15 ID.14 ID.13
ID.12 ID.11 ID.10 ID.9 ID.8 ID.7 ID.6 ID.5
ID.4 ID.3 ID.2 ID.1 ID.0 RTR Unused Unused


ID = Identifier
DB = Data Byte
ACR = TWAI_ACCEPTANCE_CODE
AMR = TWAI_ACCEPTANCE_MASK
Filter 1
ACR0 – Addr 0x0040
ACR1 – Addr 0x0044
ACR3 – Addr 0x004C
AMR0 – Addr 0x0050
AMR1 – Addr 0x0054
AMR3 – Addr 0x005C
7 6 5 4 3 2 1 0
SFF
ID.28 ID.27 ID.26 ID.25 ID.24 ID.23 ID.22 ID.21
ID.20 ID.19 ID.18 RTR DB1.7 DB1.6 DB1.5 DB1.4
DB1.3 DB1.2 DB1.1 DB1.0
EFF
ID.28 ID.27 ID.26 ID.25 ID.24 ID.23 ID.22 ID.21
ID.20 ID.19 ID.18 ID.17 ID.16 ID.15 ID.14 ID.13
Filter 2
ACR2 – Addr 0x0048
ACR3 – Addr 0x004C
AMR2 – Addr 0x0058
AMR3 – Addr 0x005C
SFF
ID.28 ID.27 ID.26 ID.25 ID.24 ID.23 ID.22 ID.21
ID.20 ID.19 ID.18 RTR
EFF
ID.28 ID.27 ID.26 ID.25 ID.24 ID.23 ID.22 ID.21
ID.20 ID.19 ID.18 ID.17 ID.16 ID.15 ID.14 ID.13


TEC, REC
0
Error Warning Limit
(default 96)
127
TEC > 255
Note 3
Error Active
Error Passive
Bus Off
Error Warning
Interrupt
Error Passive
Interrupt
Error Warning
Interrupt
Error Warning
Interrupt
Error status
0
1
Bus status
0
1
TEC : Tx Error Counter
REC : Rx Error Counter

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	1	1	2	3	3	3	3	3

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	1	1	1	1	1

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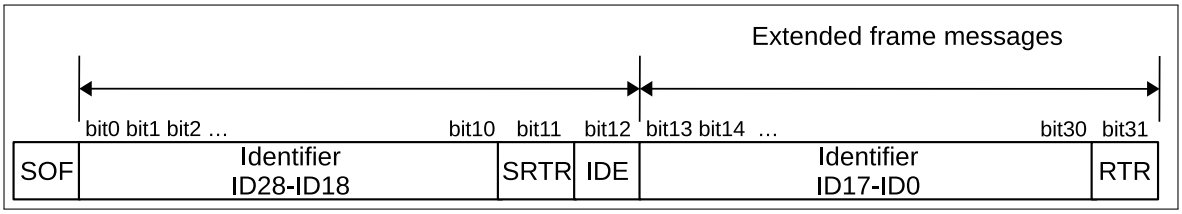
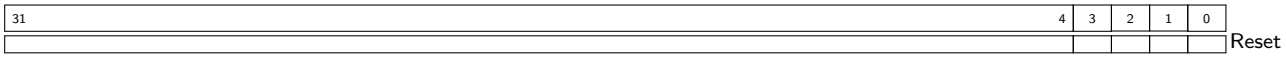
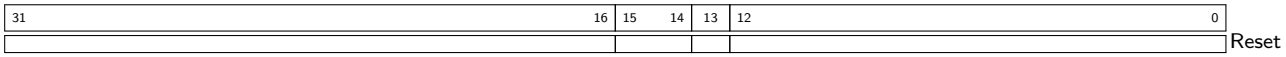
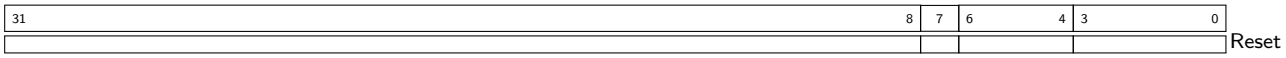
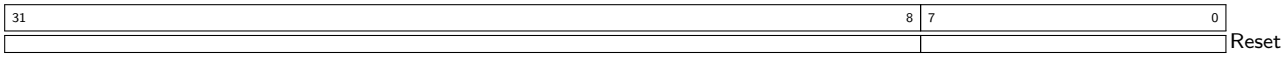
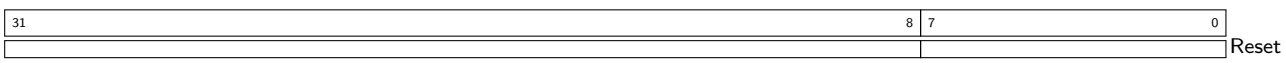

Extended frame messages
bit0 bit1 bit2 …
bit10
bit11
bit12
bit13 bit14 …
bit30
bit31
SOF
Identifier
ID28-ID18
SRTR
IDE
Identifier
ID17-ID0
RTR

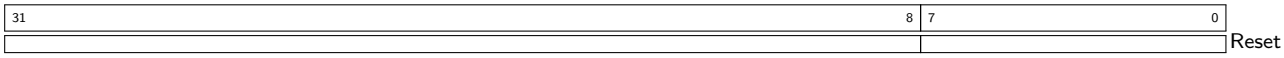

31
4
3
2
1
0
Reset

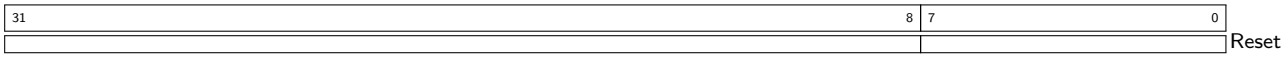

31
16
15
14
13
12
0
Reset

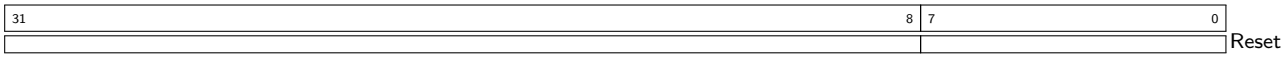

31
8
7
6
4
3
0
Reset

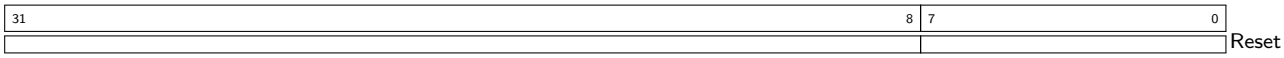

31
8
7
0
Reset


31
8
7
0
Reset


31
8
7
0
Reset


31
8
7
0
Reset


31
8
7
0
Reset


31
8
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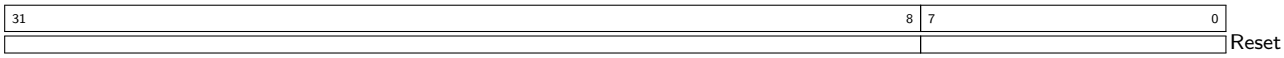
0
Reset


31
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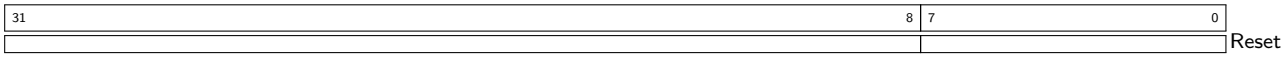
Reset


31
8
7
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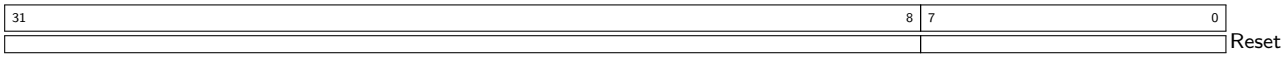
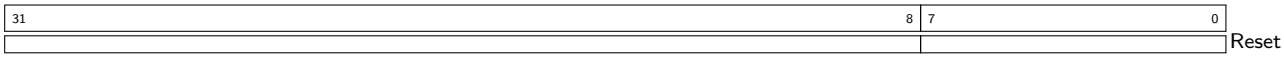
Reset


31
8
7
0
Reset


31
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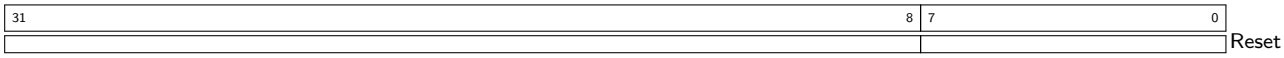
Reset


31
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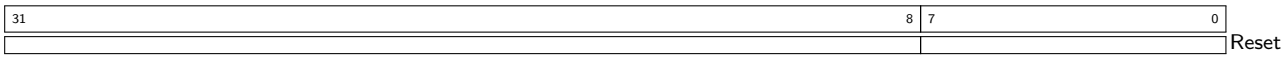
Reset


31
8
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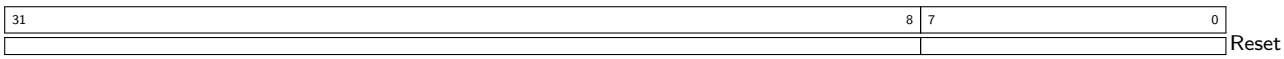
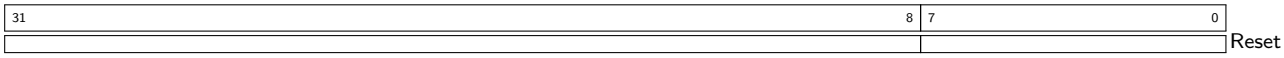
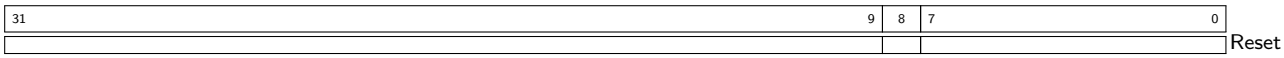
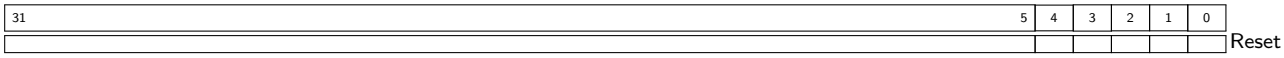
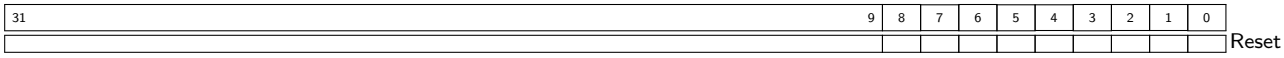
0
Reset

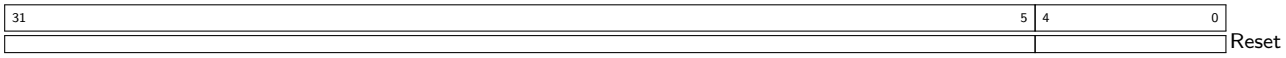

31
8
7
0
Reset

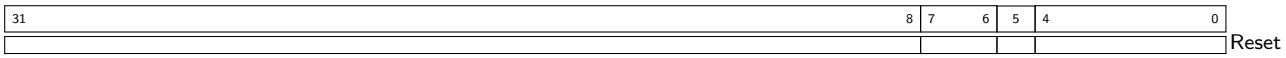

31
8
7
0
Reset

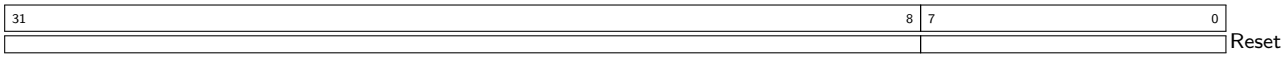

31
9
8
7
0
Reset

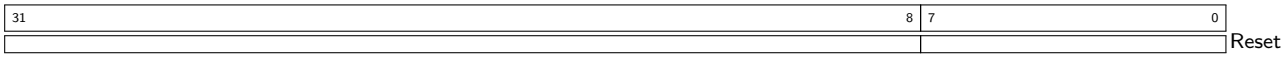

31
5
4
3
2
1
0
Reset

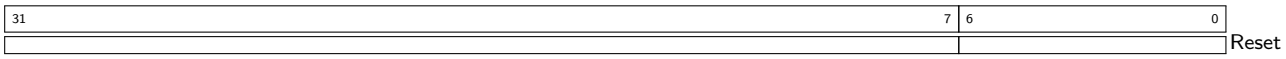

31
9
8
7
6
5
4
3
2
1
0
Reset

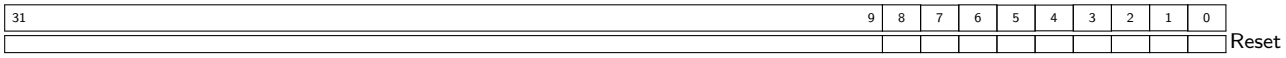

31
5
4
0
Reset

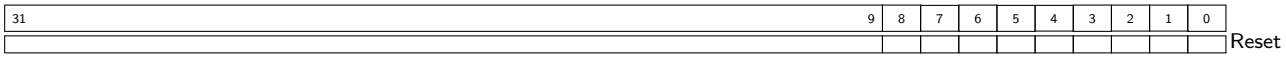

31
8
7
6
5
4
0
Reset


31
8
7
0
Reset


31
8
7
0
Reset


31
7
6
0
Reset


31
9
8
7
6
5
4
3
2
1
0
Reset


31
9
8
7
6
5
4
3
2
1
0
Reset

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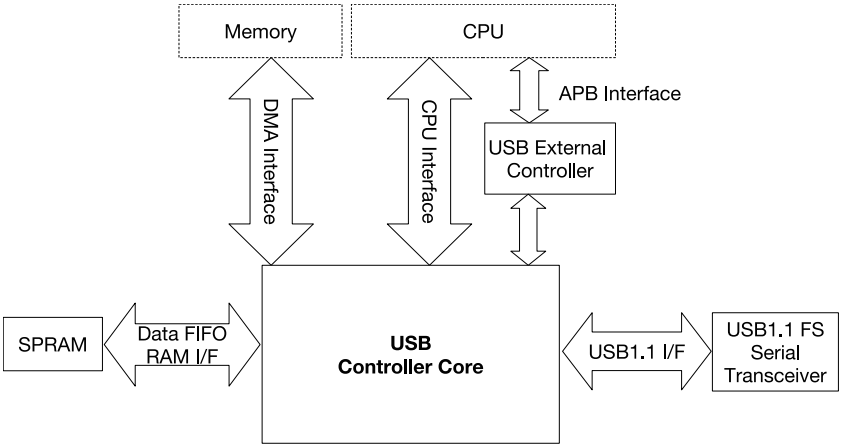
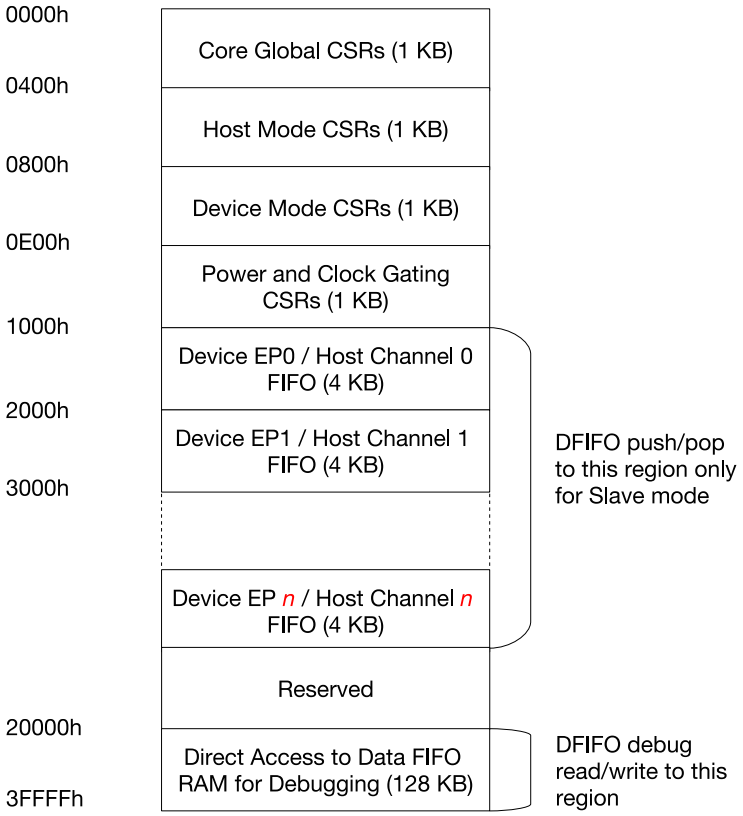

Memory
CPU
APB Interface
DMA Interface
CPU Interface
USB External Controller
SPRAM
Data FIFO RAM I/F
USB Controller Core
USB1.1 I/F
USB1.1 FS Serial Transceiver


0000h
Core Global CSRs (1 KB)
0400h
Host Mode CSRs (1 KB)
0800h
Device Mode CSRs (1 KB)
0E00h
Power and Clock Gating CSRs (1 KB)
1000h
Device EP0 / Host Channel 0 FIFO (4 KB)
2000h
Device EP1 / Host Channel 1 FIFO (4 KB)
3000h
Device EP n / Host Channel n FIFO (4 KB)
Reserved
20000h
Direct Access to Data FIFO RAM for Debugging (128 KB)
3FFFFh
DFIFO push/pop to this region only for Slave mode
DFIFO debug read/write to this region

-
-
-
-
-
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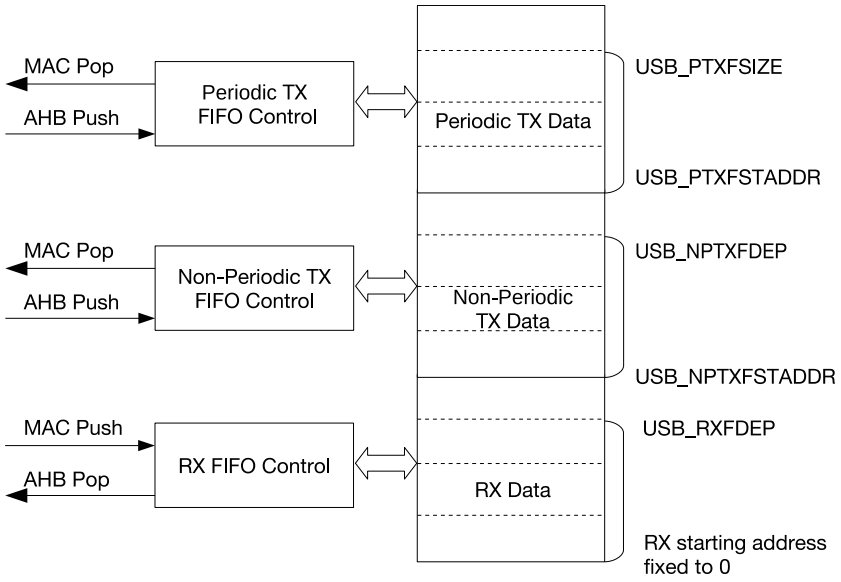
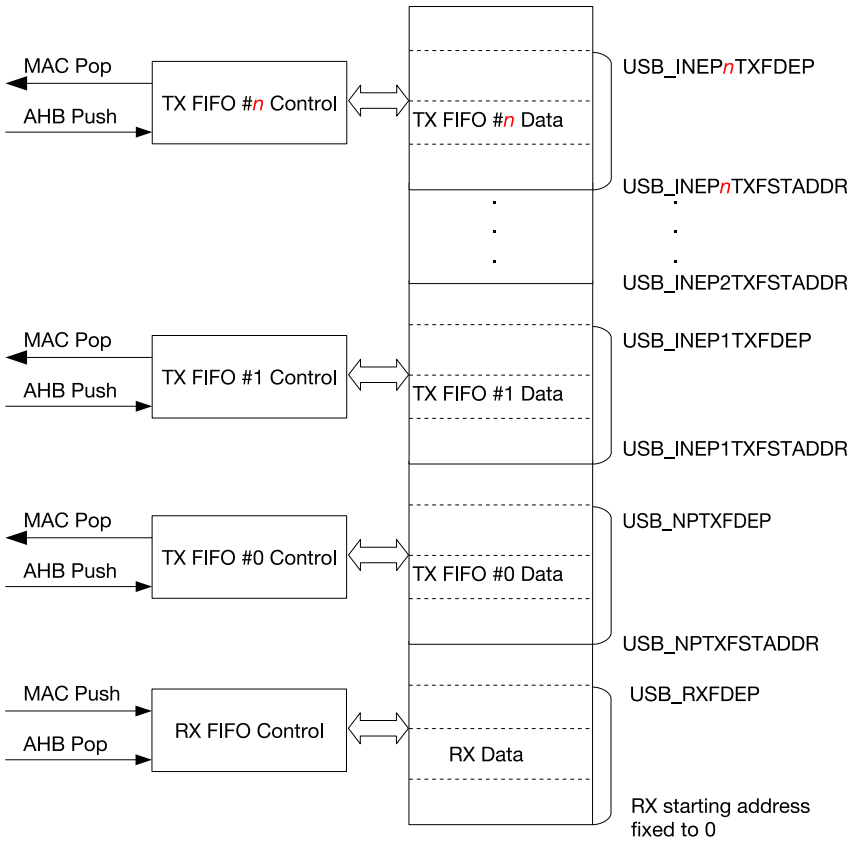
-
-


MAC Pop
AHB Push
Periodic TX
FIFO Control
Periodic TX Data
USB_PTXFSIZE
USB_PTXFSTADDR
MAC Pop
AHB Push
Non-Periodic TX
FIFO Control
Non-Periodic
TX Data
USB_NPTXFDEP
USB_NPTXFSTADDR
MAC Push
AHB Pop
RX FIFO Control
RX Data
USB_RXFDEP
RX starting address
fixed to 0

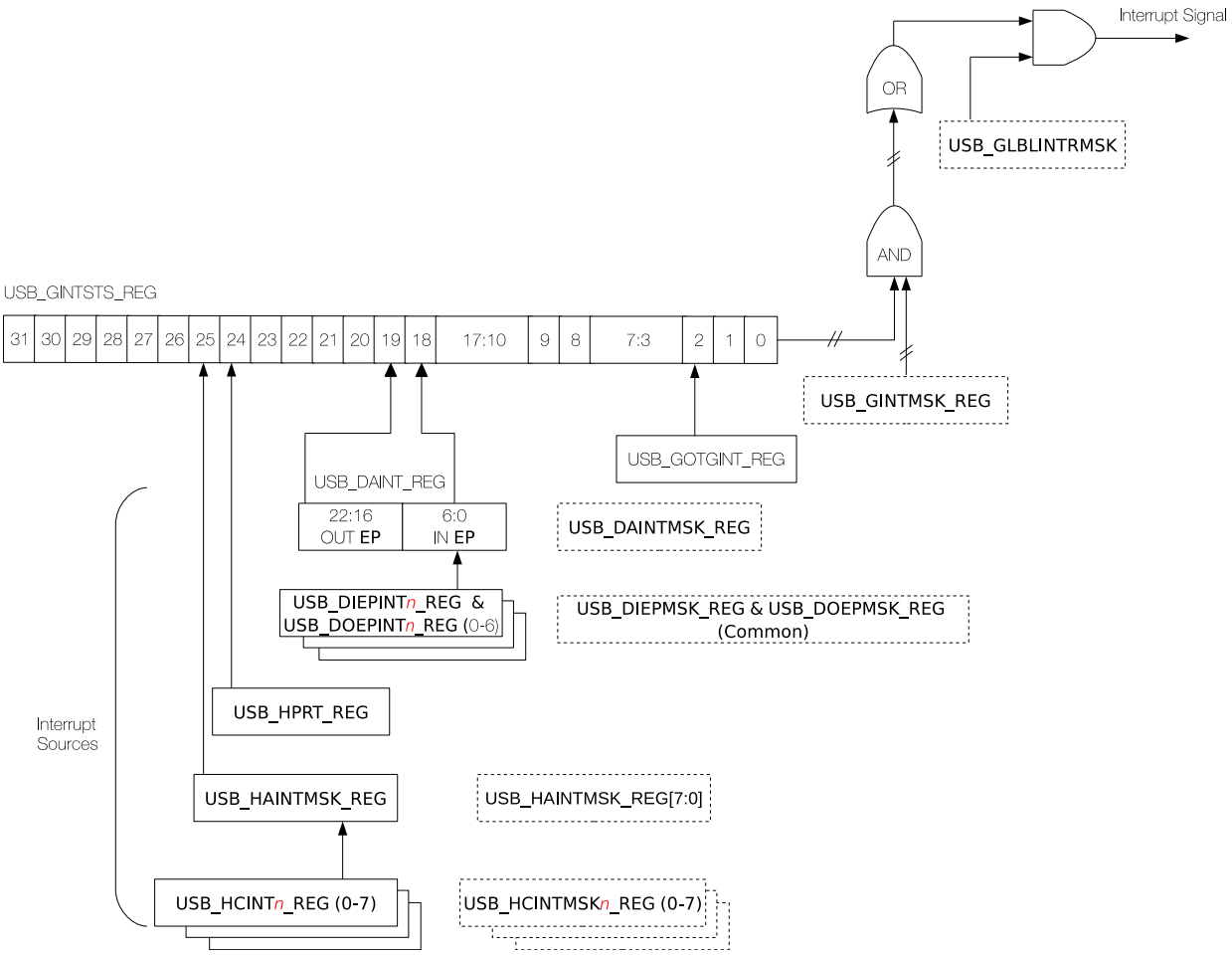
-
-

-
-

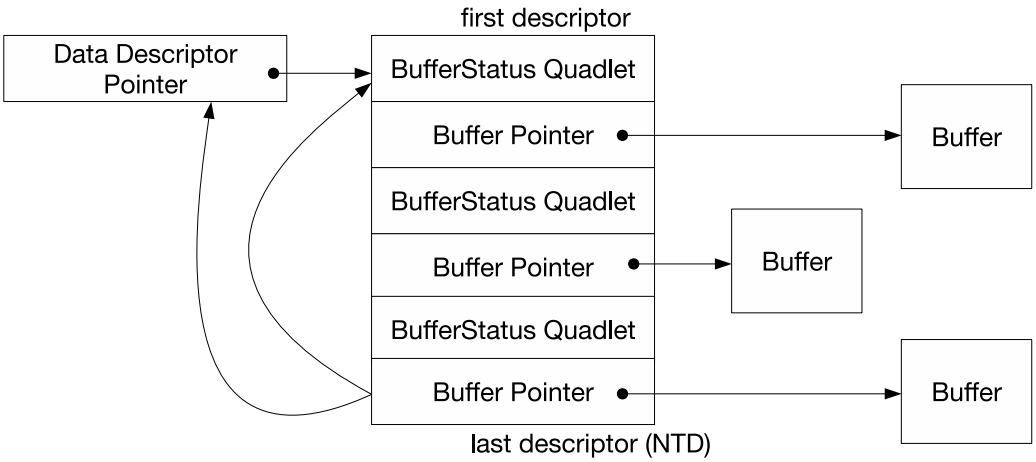

MAC Pop
AHB Push
TX FIFO #n Control
TX FIFO #n Data
USB_INEPnTXFDEP
USB_INEPnTXFSTADDR
USB_INEP2TXFSTADDR
MAC Pop
AHB Push
TX FIFO #1 Control
TX FIFO #1 Data
USB_INEP1TXFDEP
USB_INEP1TXFSTADDR
MAC Pop
AHB Push
TX FIFO #0 Control
TX FIFO #0 Data
USB_NPTXFDEP
USB_NPTXFSTADDR
MAC Push
AHB Pop
RX FIFO Control
RX Data
USB_RXFDEP
RX starting address
fixed to 0

-
-
-
-
-

-
-


Interrupt Signal
OR
USB_GLBLINTRMSK
AND
USB_GINTSTS_REG
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17:10 9 8 7:3 2 1 0
USB_GINTMSK_REG
USB_DAINT_REG
22:16 OUT EP
6:0 IN EP
USB_GOTGINT_REG
USB_DAINTMSK_REG
USB_DIEPINTn_REG & USB_DOEPINTn_REG (0-6)
USB_DIEPMSK_REG & USB_DOEPMSK_REG (Common)
Interrupt Sources
USB_HPRT_REG
USB_HAINTMSK_REG
USB_HAINTMSK_REG[7:0]
USB_HCINTn_REG (0-7)
USB_HCINTMSKn_REG (0-7)

-
-


first descriptor
Data Descriptor Pointer
BufferStatus Quadlet
Buffer Pointer
Buffer
BufferStatus Quadlet
Buffer Pointer
Buffer
BufferStatus Quadlet
Buffer Pointer
Buffer
last descriptor (NTD)

-
-

-
-
-
-

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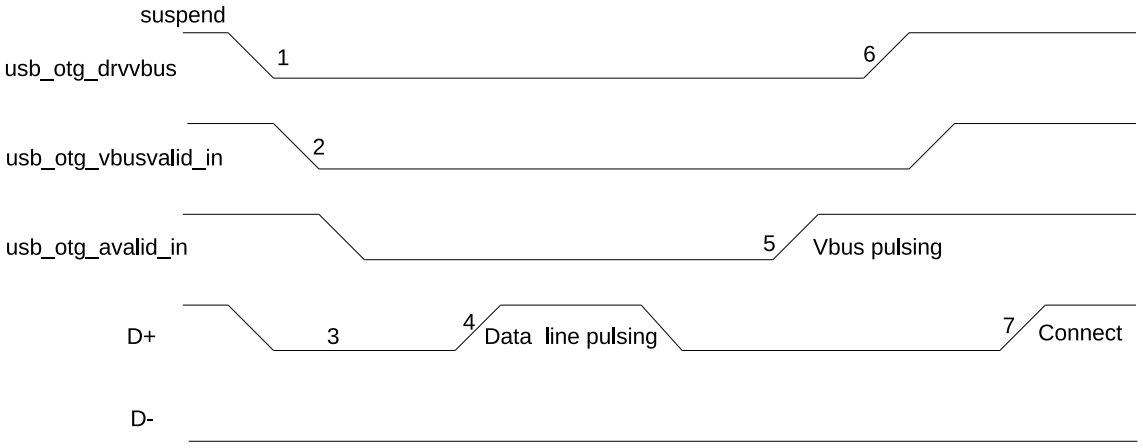
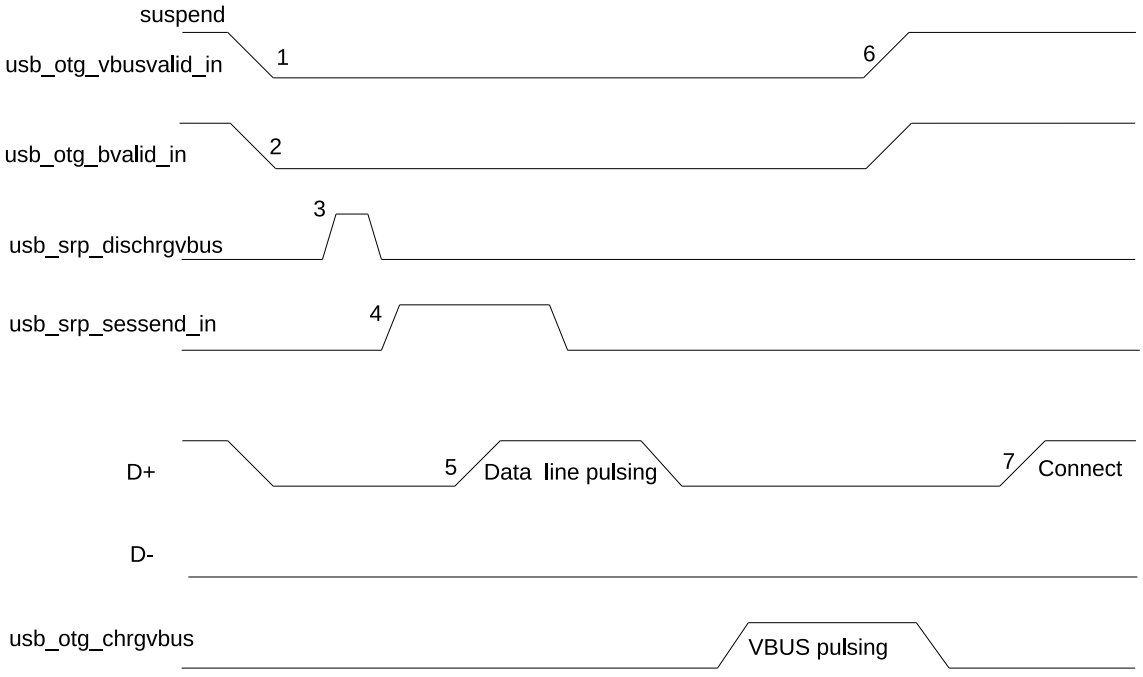
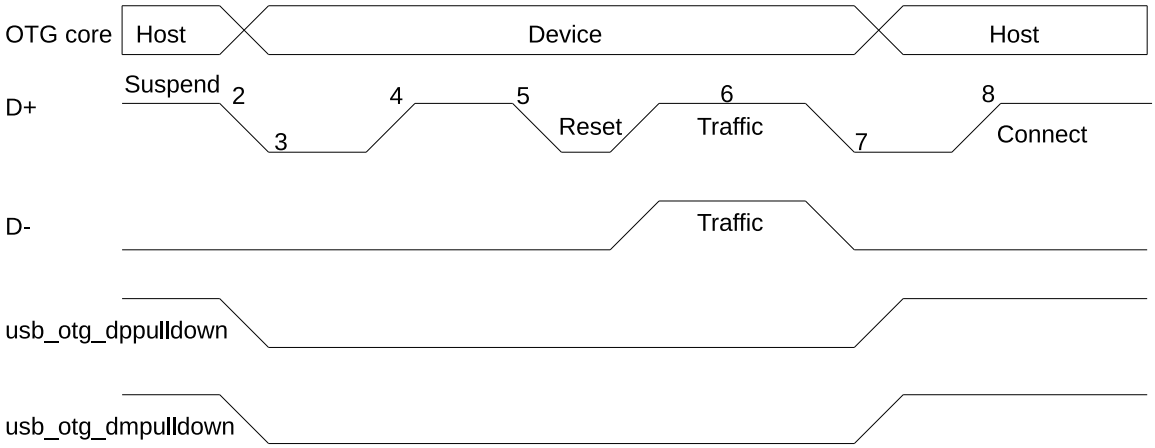
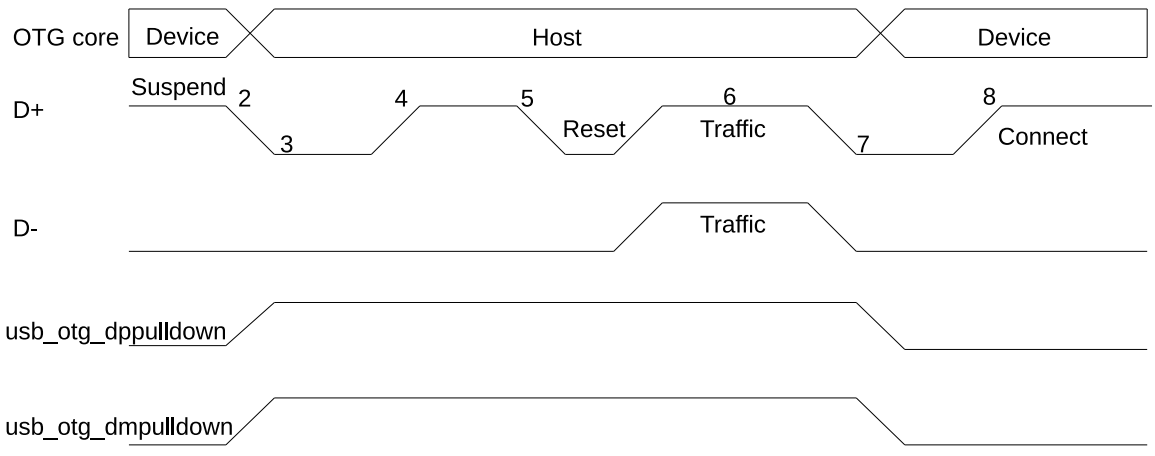
		Ω

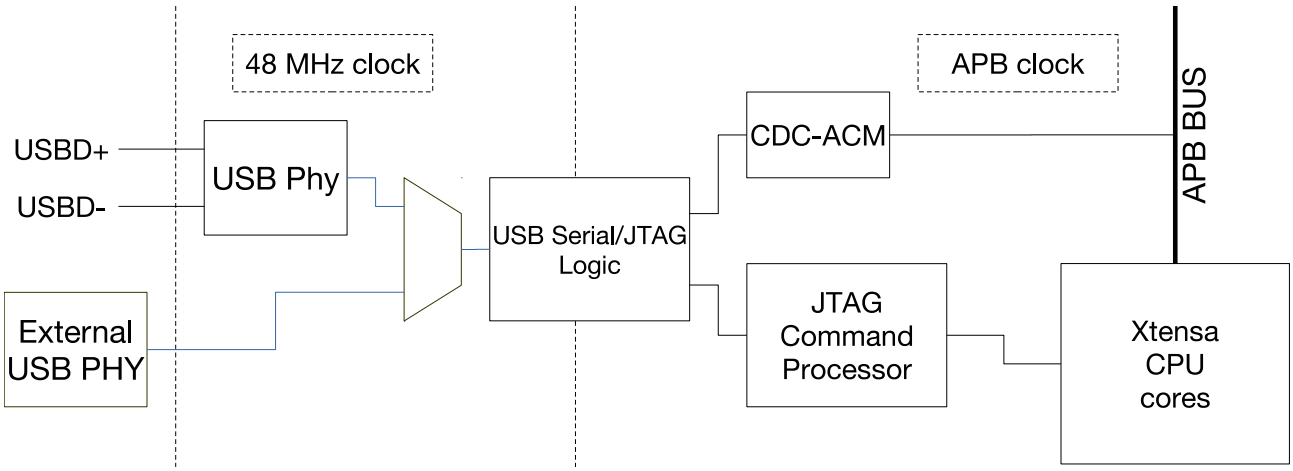

suspend
usb_otg_drvvbus
1
6
usb_otg_vbusvalid_in
2
usb_otg_avalid_in
5
Vbus pulsing
D+
3
4
Data line pulsing
7
Connect
D-

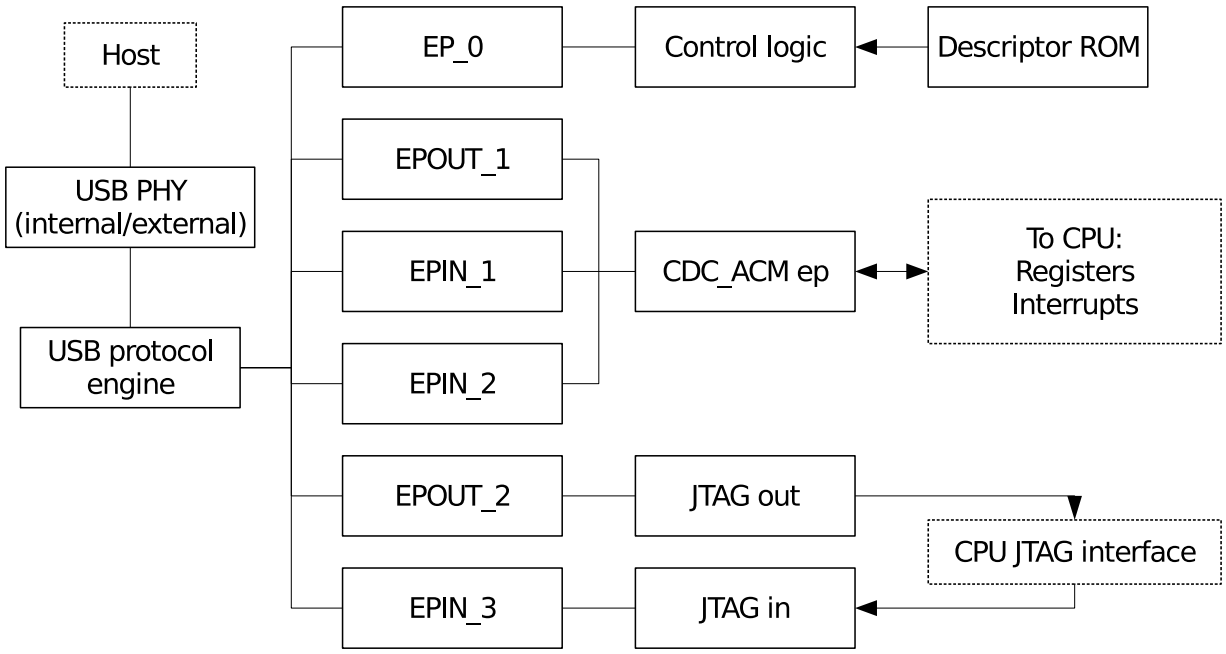

suspend
usb_otg_vbusvalid_in
1
6
usb_otg_bvalid_in
2
3
usb_srp_dischrgvbus
usb_srp_sessend_in
4
D+
5
Data line pulsing
7
Connect
D-
usb_otg_chrgvbus
VBUS pulsing

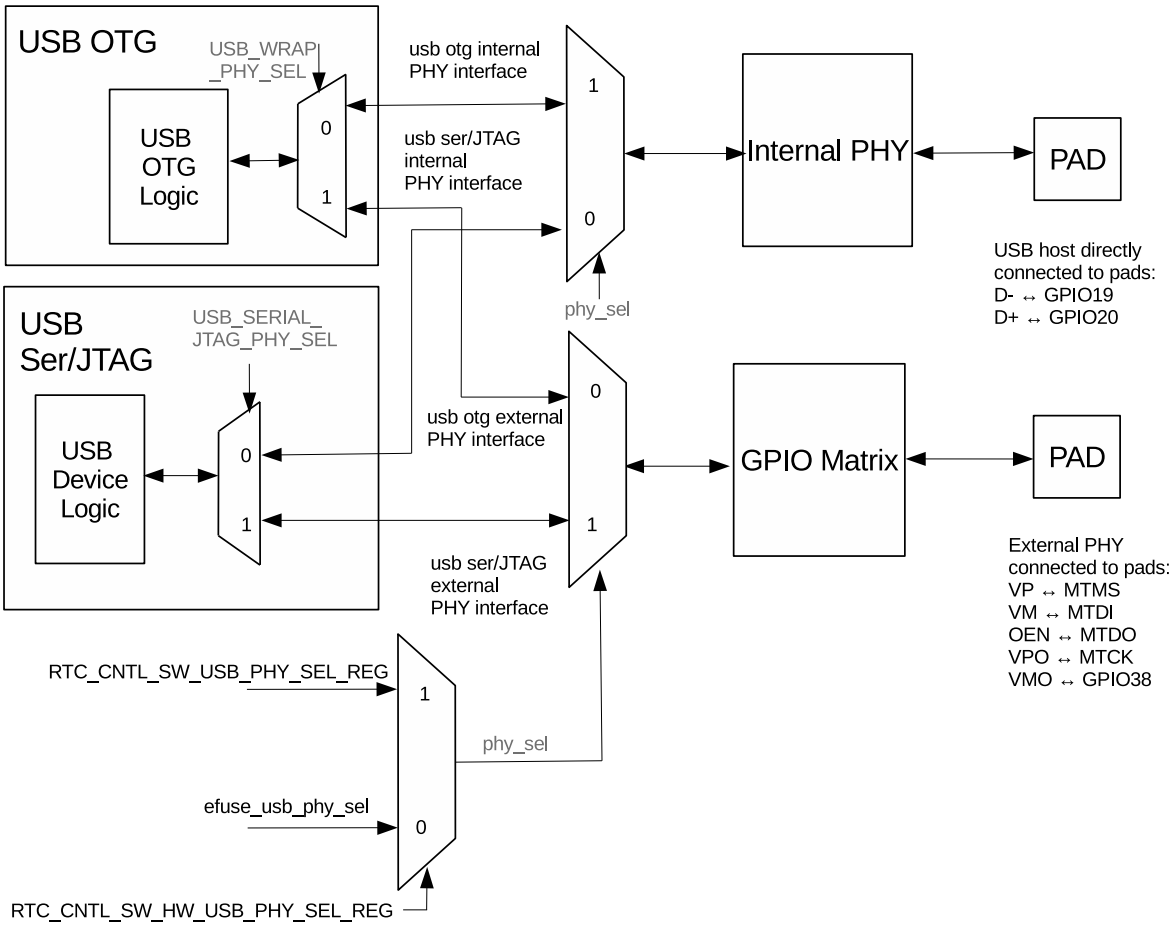

OTG core
Host
Device
Host
D+
Suspend
2
3
4
5
Reset
6
Traffic
7
8
Connect
D-
Traffic
usb_otg_dppulldown
usb_otg_dmpulldown

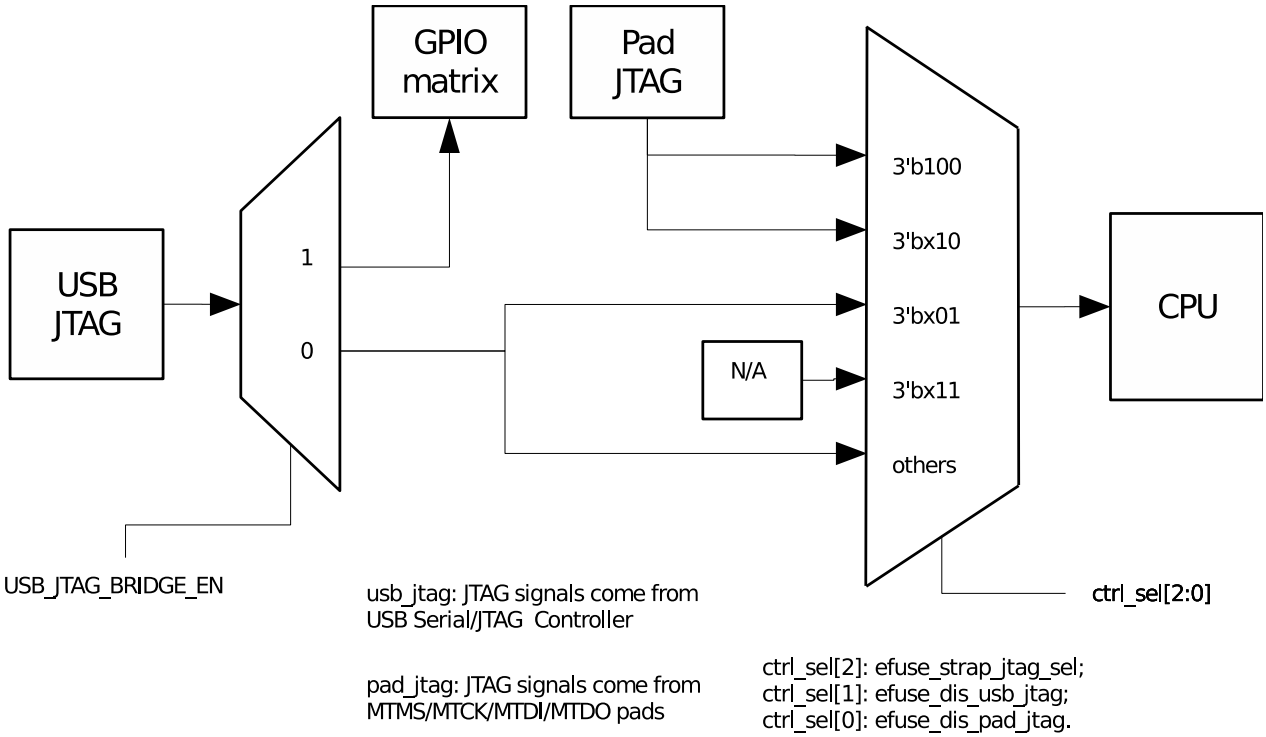

OTG core
Device
Host
Device
D+
Suspend
2
3
4
5
Reset
6
Traffic
7
8
Connect
D-
Traffic
usb_otg_dppulldown
usb_otg_dmpulldown

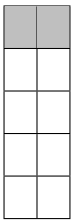
-
-
-
-
-
-
-
-


48 MHz clock
APB clock
USBD+
USBD-
USB Phy
CDC-ACM
APB BUS
USB Serial/JTAG Logic
External USB PHY
JTAG Command Processor
Xtensa CPU cores


Host
USB PHY
(internal/external)
USB protocol
engine
EP_0
EPOUT_1
EPIN_1
EPIN_2
EPOUT_2
EPIN_3
Control logic
Descriptor ROM
CDC_ACM ep
To CPU:
Registers
Interrupts
JTAG out
CPU JTAG interface
JTAG in


USB OTG
USB_WRAP
_PHY_SEL
USB
OTG
Logic
0
1
usb otg internal
PHY interface
usb ser/JTAG
internal
PHY interface
1
0
Internal PHY
PAD
USB host directly
connected to pads:
D- ↔ GPIO19
D+ ↔ GPIO20
phy_sel
USB
Ser/JTAG
USB_SERIAL_
JTAG_PHY_SEL
USB
Device
Logic
0
1
usb otg external
PHY interface
0
1
GPIO Matrix
PAD
External PHY
connected to pads:
VP ↔ MTMS
VM ↔ MTDI
OEN ↔ MTDO
VPO ↔ MTCK
VMO ↔ GPIO38
usb ser/JTAG
external
PHY interface
RTC_CNTL_SW_USB_PHY_SEL_REG
1
phy_sel
efuse_usb_phy_sel
0
RTC_CNTL_SW_HW_USB_PHY_SEL_REG


GPIO matrix
Pad JTAG
USB JTAG
1
0
3'b100
3'bx10
3'bx01
3'bx11
others
N/A
CPU
USB_JTAG_BRIDGE_EN
usb_jtag: JTAG signals come from USB Serial/JTAG Controller
pad_jtag: JTAG signals come from MTMS/MTCK/MTDI/MTDO pads
ctrl_sel[2:0]
ctrl_sel[2]: efuse_strap_jtag_sel;
ctrl_sel[1]: efuse_dis_usb_jtag;
ctrl_sel[0]: efuse_dis_pad_jtag.



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-
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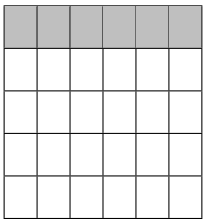
-
- $norepetitions = (R1 \times 2 + R0) \times (4^{cmdrepcount})$

$(0 \times 2 + 1) \times (4^0) = 1$

$(1 \times 2 + 0) \times (4^0) = 2$

$(0 \times 2 + 0) \times (4^1) = 0$

$(1 \times 2 + 1) \times (4^2) = 48$



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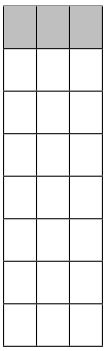
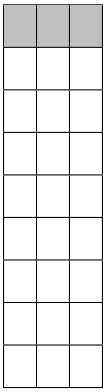
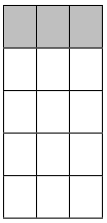
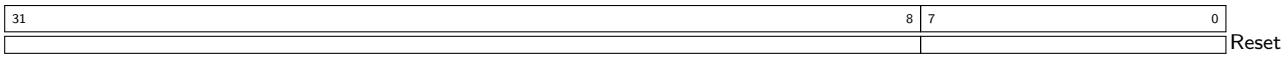
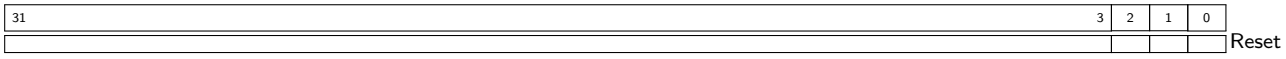







31
8
7
0
Reset


31
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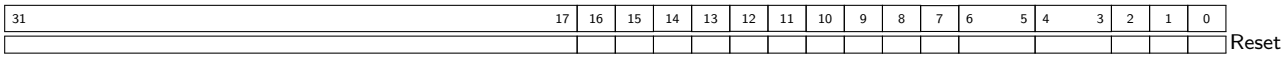
Reset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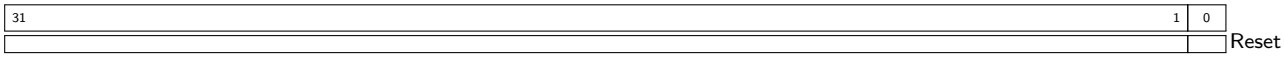
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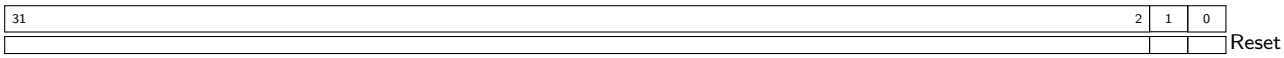
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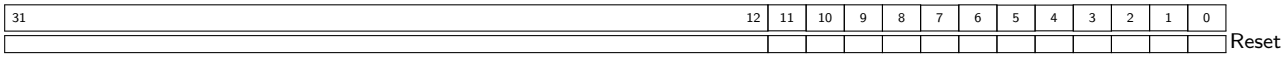
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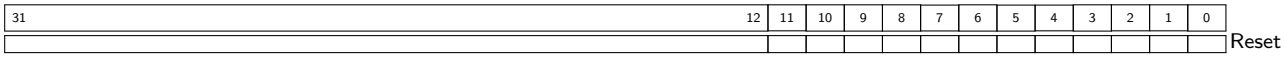
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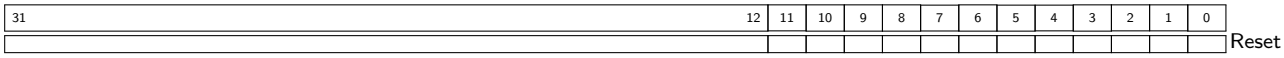
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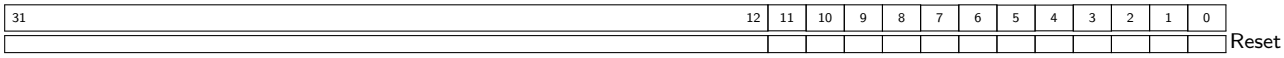
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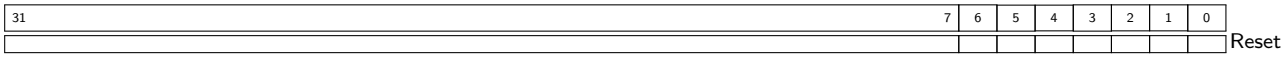
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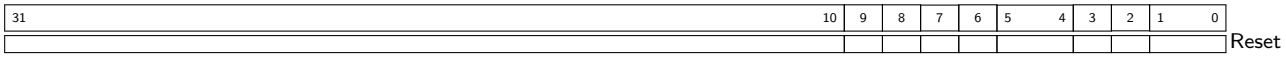
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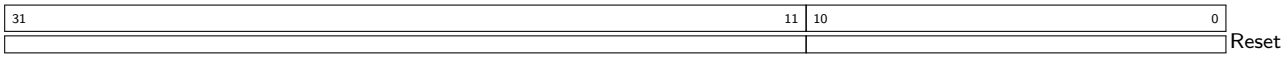
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11
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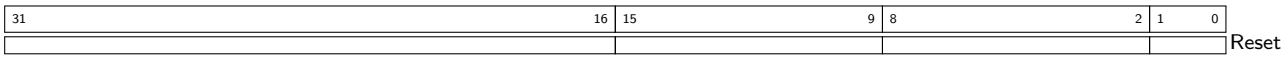
Reset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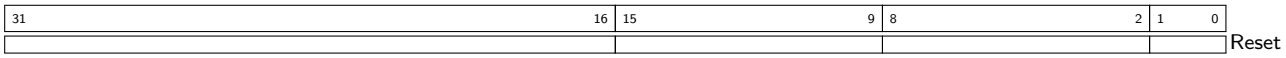
Reset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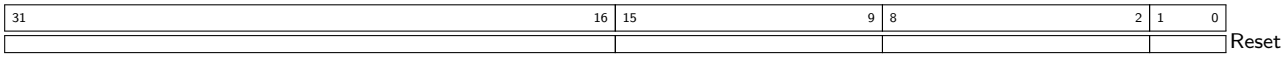
Reset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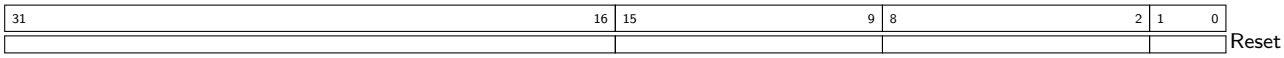
Reset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16
15
9
8
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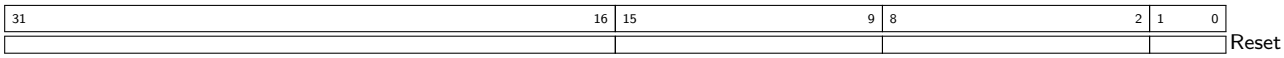
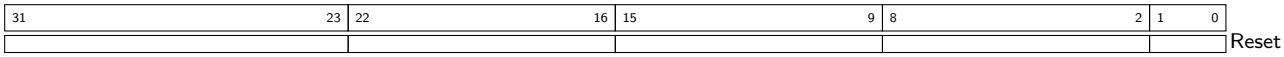
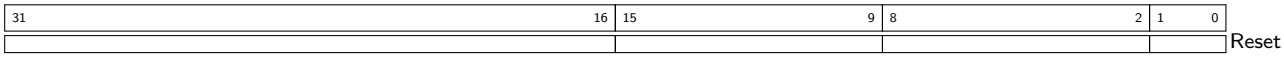
Reset


31
16
15
9
8
2
1
0
Reset


31
23
22
16
15
9
8
2
1
0
Reset


31
16
15
9
8
2
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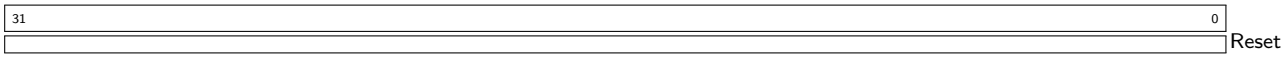
0
Reset


31
0
Reset

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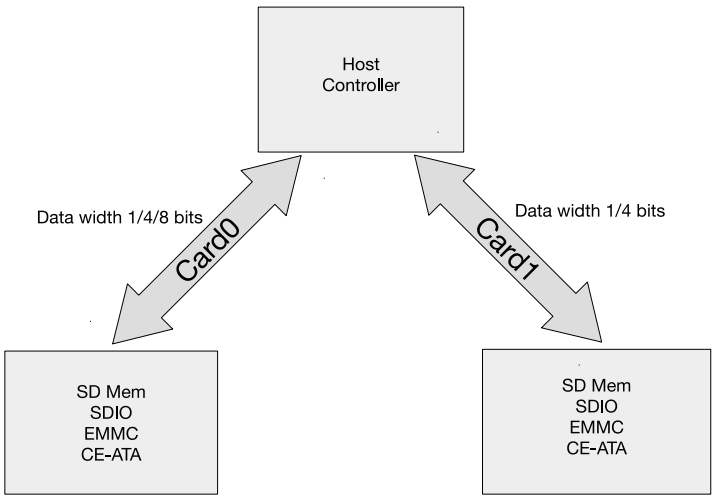
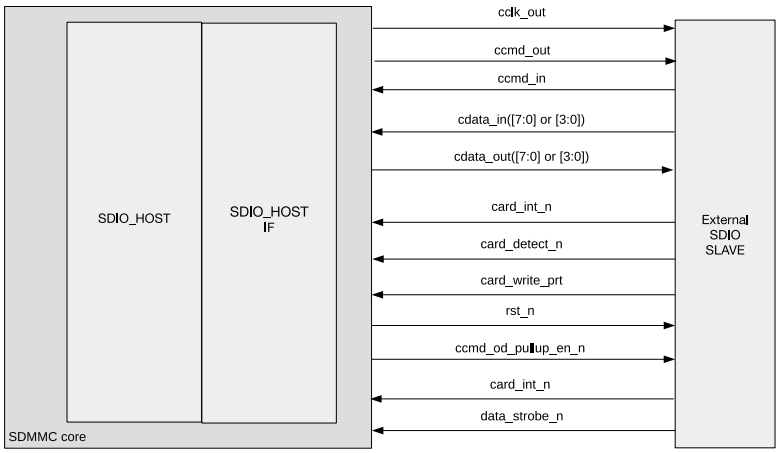
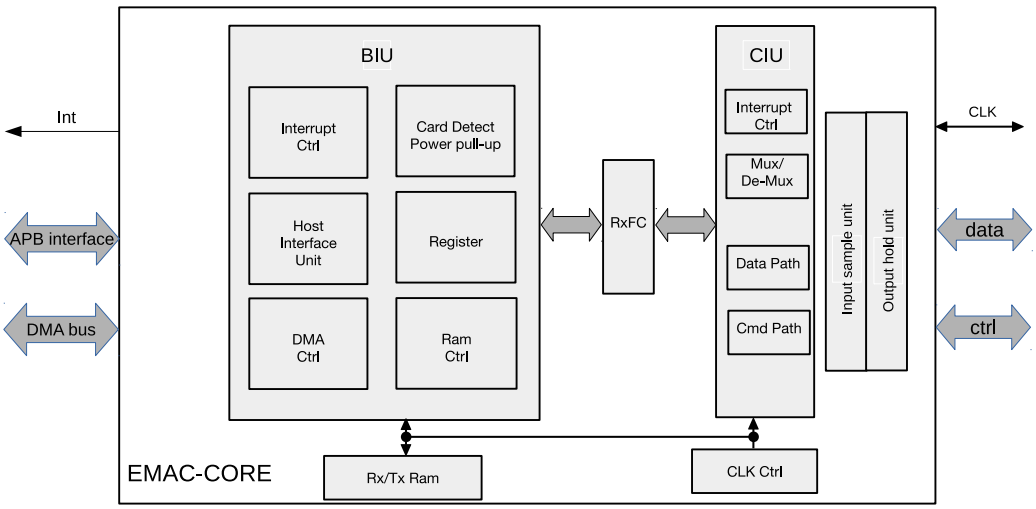

Host
Controller
Data width 1/4/8 bits
Card0
Data width 1/4 bits
Card1
SD Mem
SDIO
EMMC
CE-ATA
SD Mem
SDIO
EMMC
CE-ATA


SDIO_HOST
SDIO_HOST IF
SDMMC core
cclk_out
ccmd_out
ccmd_in
cdata_in([7:0] or [3:0])
cdata_out([7:0] or [3:0])
card_int_n
card_detect_n
card_write_prt
rst_n
ccmd_od_pullup_en_n
card_int_n
data_strobe_n
External SDIO SLAVE

-
-


Int
APB interface
DMA bus
BIU
Interrupt Ctrl
Card Detect Power pull-up
Host Interface Unit
Register
DMA Ctrl
Ram Ctrl
RxFC
CIU
Interrupt Ctrl
Mux/ De-Mux
Data Path
Cmd Path
Input sample unit
Output hold unit
CLK
data
ctrl
EMAC-CORE
Rx/Tx Ram
CLK Ctrl

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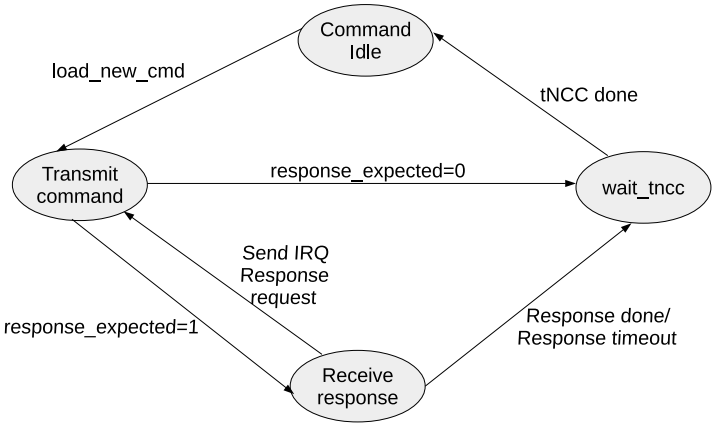
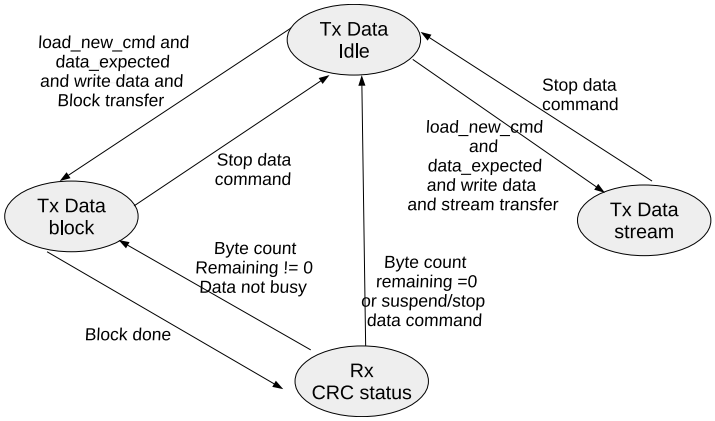
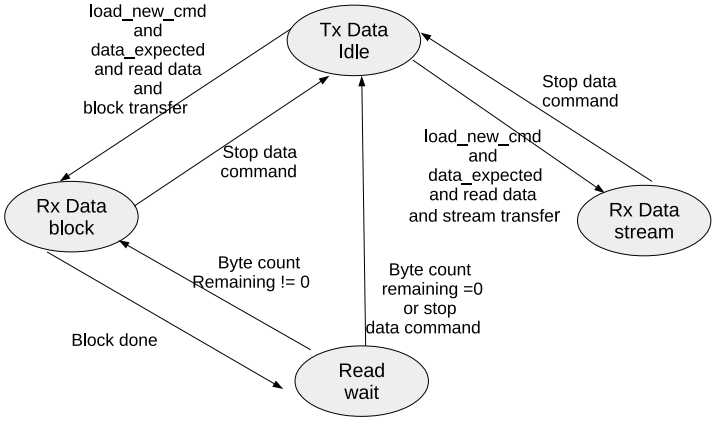

Command
Idle
load_new_cmd
tNCC done
Transmit
command
response_expected=0
wait_tncc
Send IRQ
Response
request
response_expected=1
Response done/
Response timeout
Receive
response

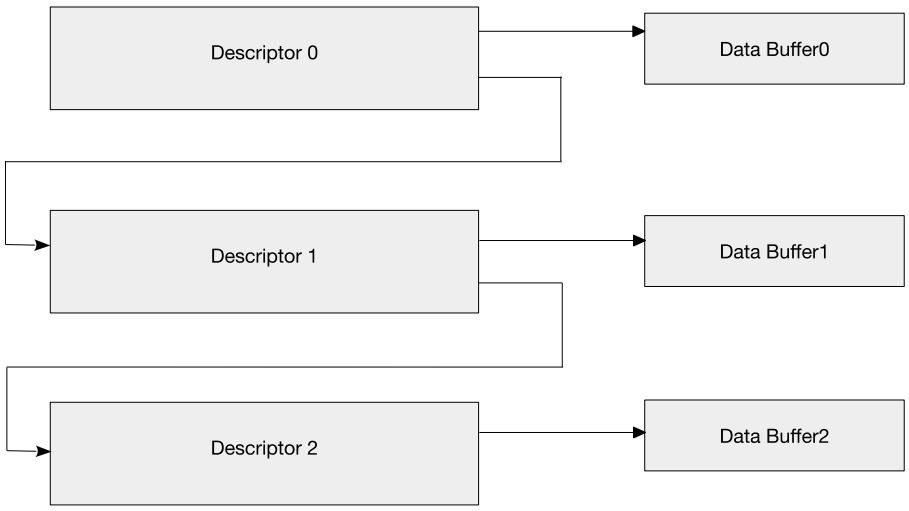
-
-

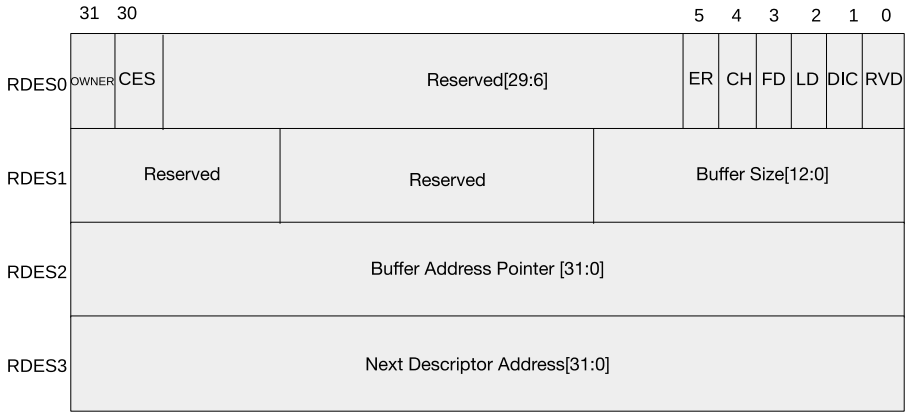

Tx Data
Idle
load_new_cmd and
data_expected
and write data and
Block transfer
Stop data
command
load_new_cmd
and
data_expected
and write data
and stream transfer
Stop data
command
Tx Data
block
Tx Data
stream
Byte count
Remaining != 0
Data not busy
Byte count
remaining =0
or suspend/stop
data command
Block done
Rx
CRC status


load_new_cmd
and
data_expected
and read data
and
block transfer
Tx Data
Idle
Stop data
command
load_new_cmd
and
data_expected
and read data
and stream transfer
Rx Data
stream
Stop data
command
Rx Data
block
Byte count
Remaining != 0
Byte count
remaining =0
or stop
data command
Block done
Read
wait

-
-
-
-
-
-
-
-
-
-
-
-

-
-
-
-
-
-
-
-
-
-


Descriptor 0
Data Buffer0
Descriptor 1
Data Buffer1
Descriptor 2
Data Buffer2



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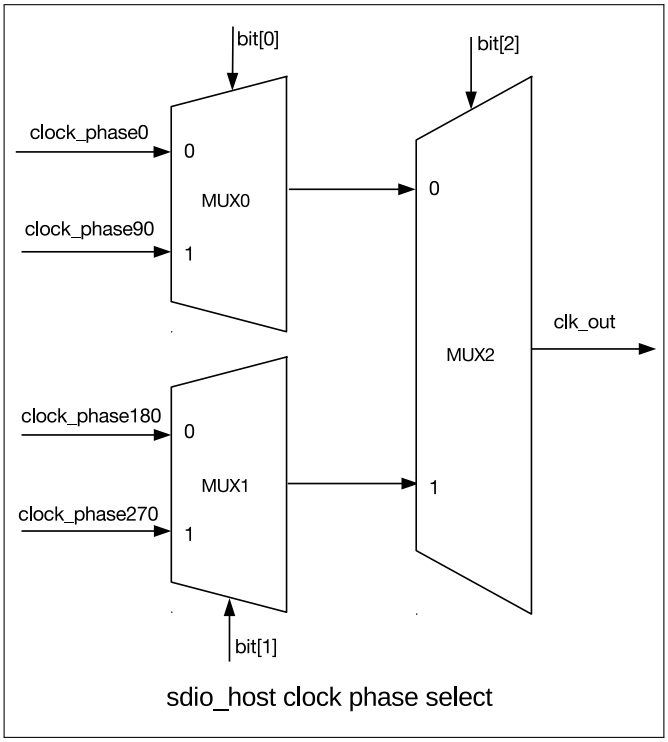
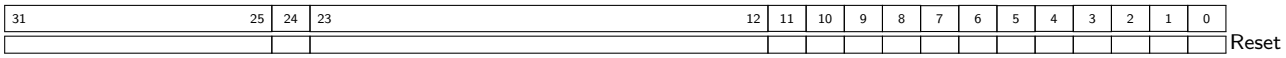


sdio_host clock phase select


31
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12
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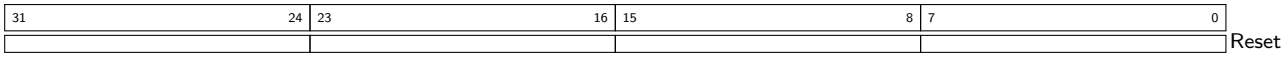
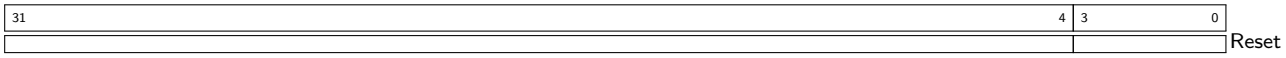
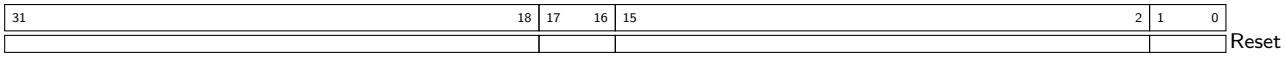
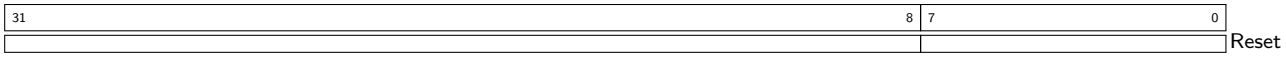
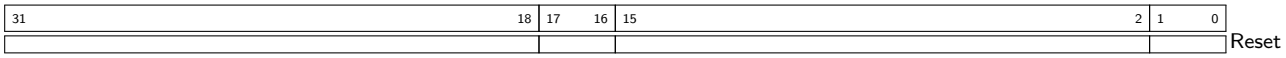
0
Reset


31
24
23
16
15
8
7
0
Reset


31
4
3
0
Reset


31
18
17
16
15
2
1
0
Reset


31
8
7
0
Reset


31
18
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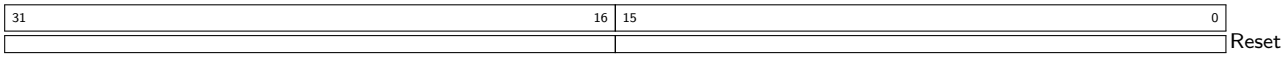
Reset


31
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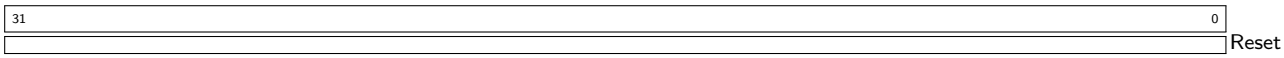
Reset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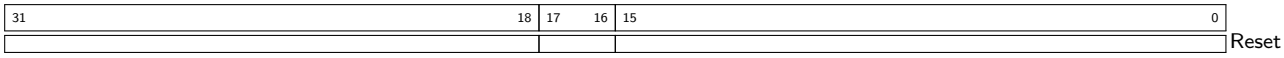
Reset


31
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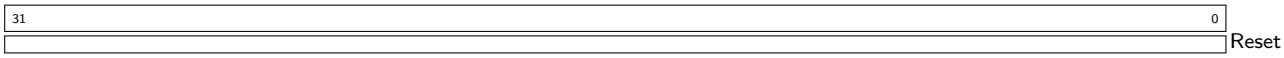
Reset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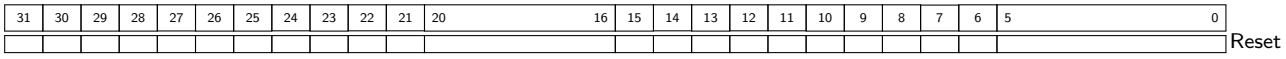
Reset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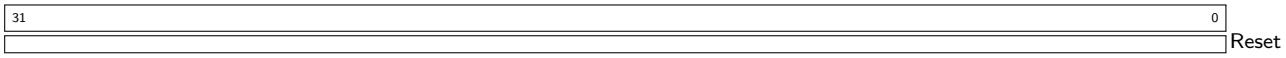
Reset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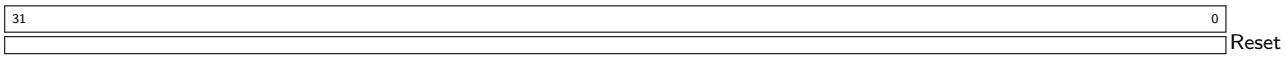
Reset


31
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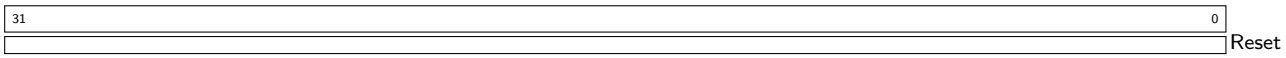
Reset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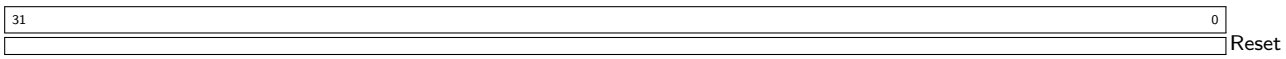
Reset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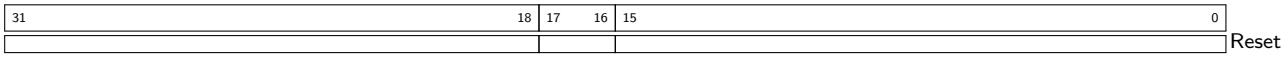
Reset


31
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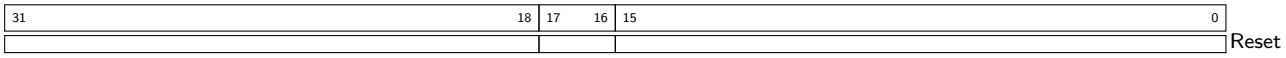
Reset


31
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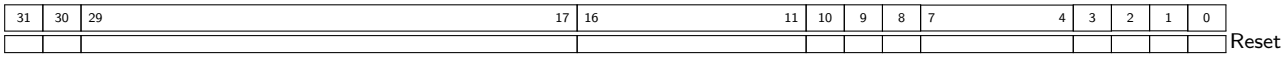
Reset


31
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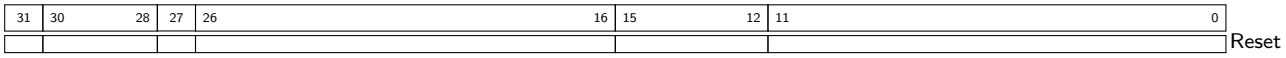
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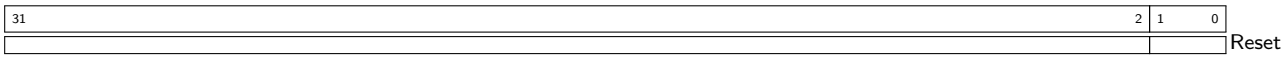
Reset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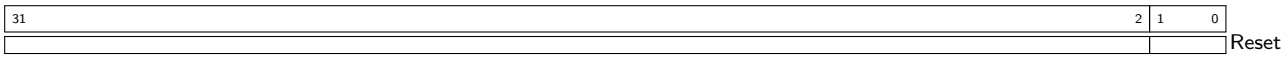
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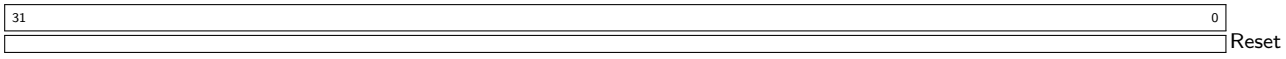
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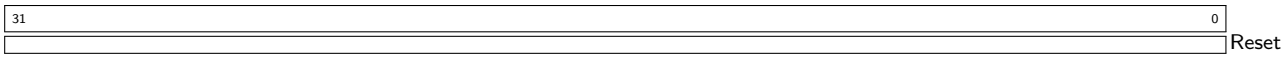
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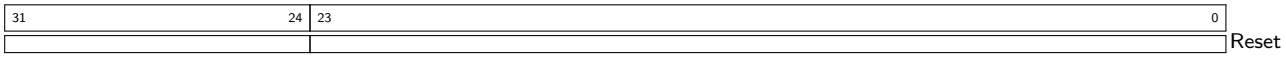
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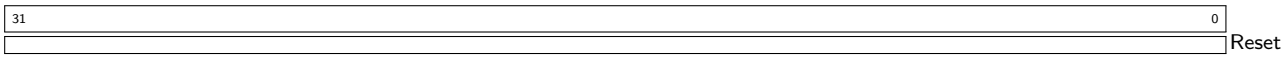
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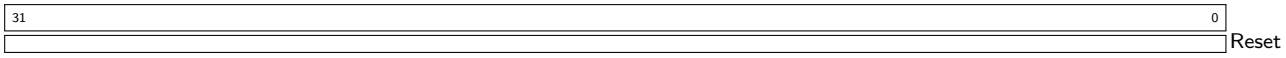
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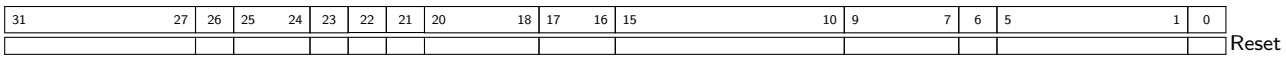
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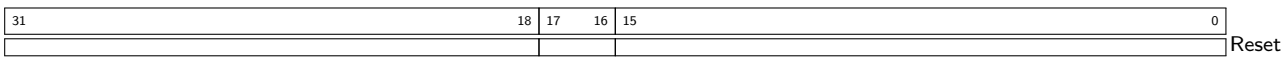
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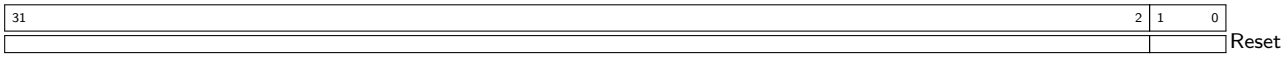
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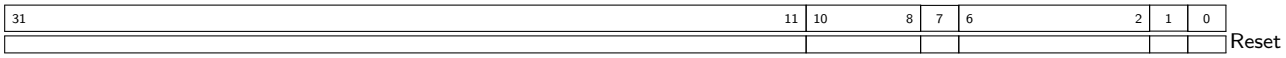
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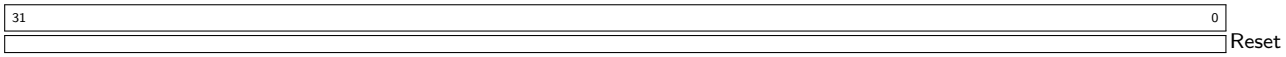
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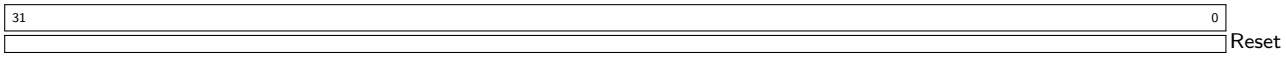
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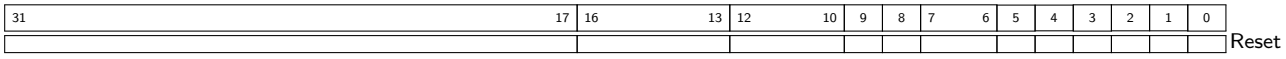
Reset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17
16
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10
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8
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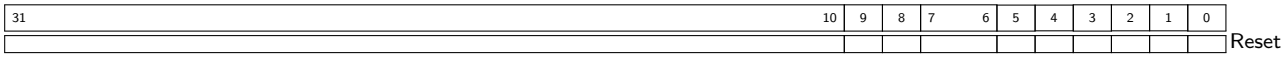
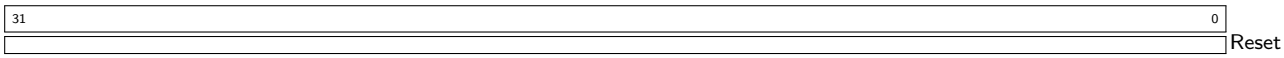
6
5
4
3
2
1
0
Reset


31
10
9
8
7
6
5
4
3
2
1
0
Reset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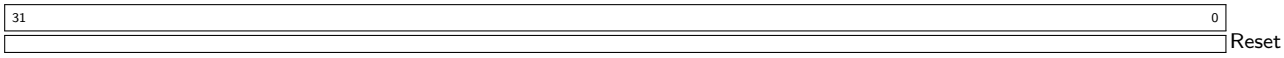
Reset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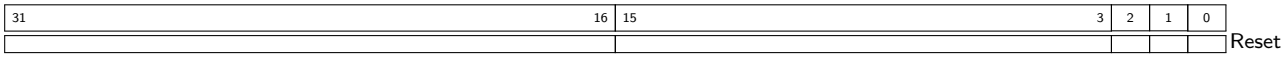
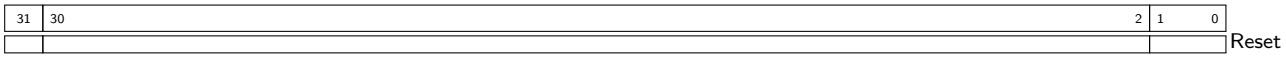
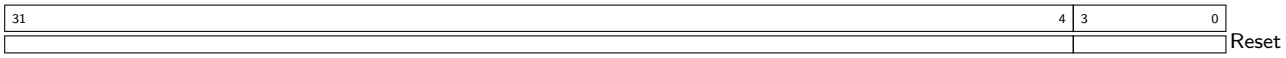
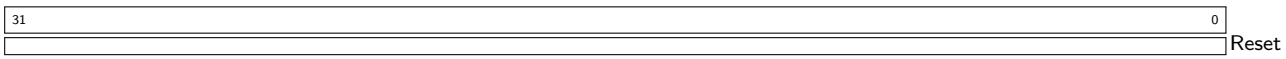
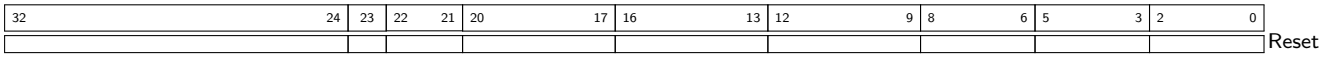
Reset


31
16
15
3
2
1
0
Reset


31
30
2
1
0
Reset


31
4
3
0
Reset


31
0
Reset


32 24
23
22 21
20 17
16 13
12 9
8 6
5 3
2 0
Reset

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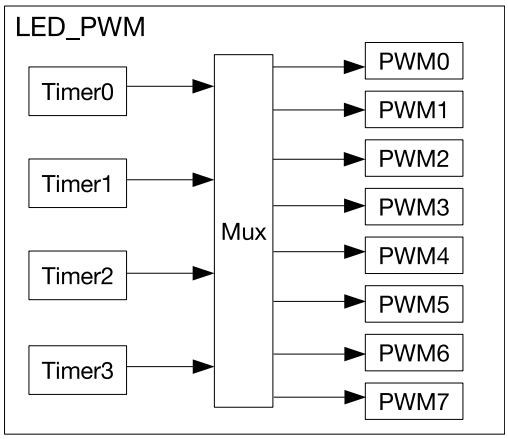
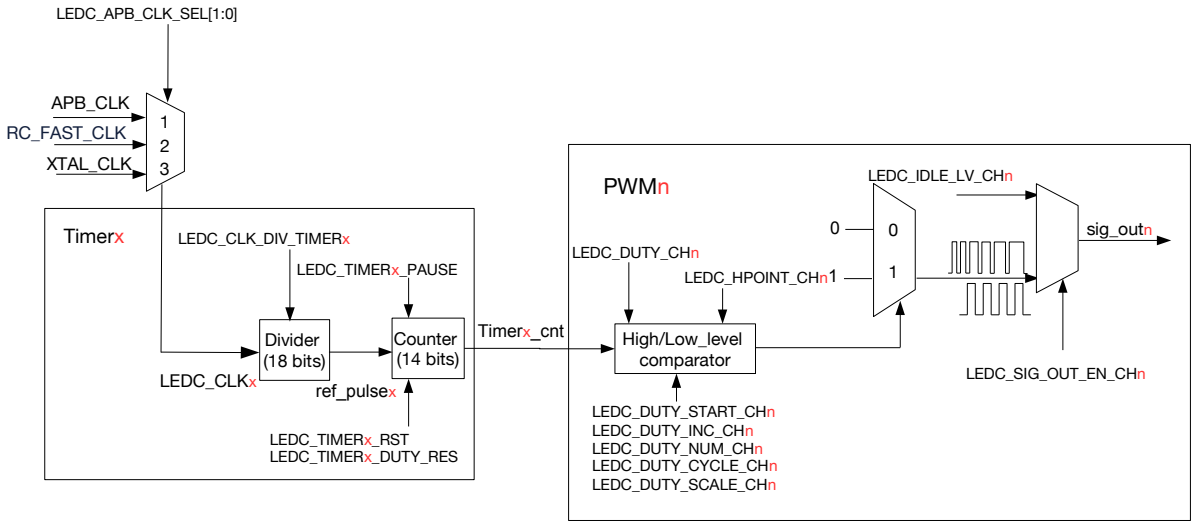
-


LED_PWM
Timer0
Timer1
Timer2
Timer3
Mux
PWM0
PWM1
PWM2
PWM3
PWM4
PWM5
PWM6
PWM7



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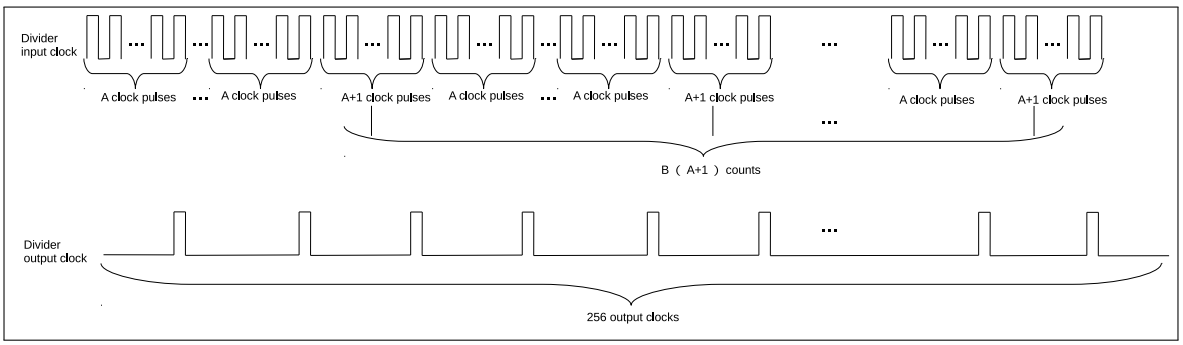
-

$$LEDCCLKDIV = A + \frac{B}{256}$$

-
-

-

-
-



$2^{LEDCTIMERDUTYRES} - 1$

$LEDCOVFNUMCH + 1$

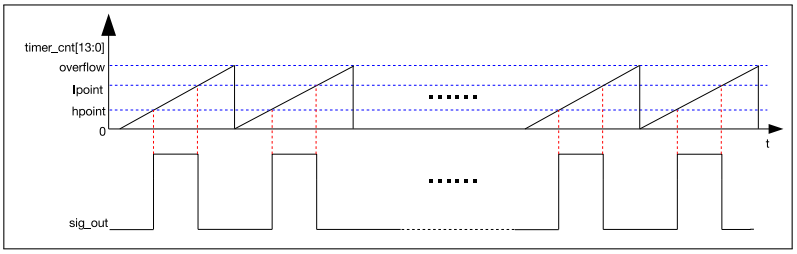
$$f = \frac{f}{\cdot 2}$$

$$= {}_2\left(\frac{f}{f\cdot}\right)$$

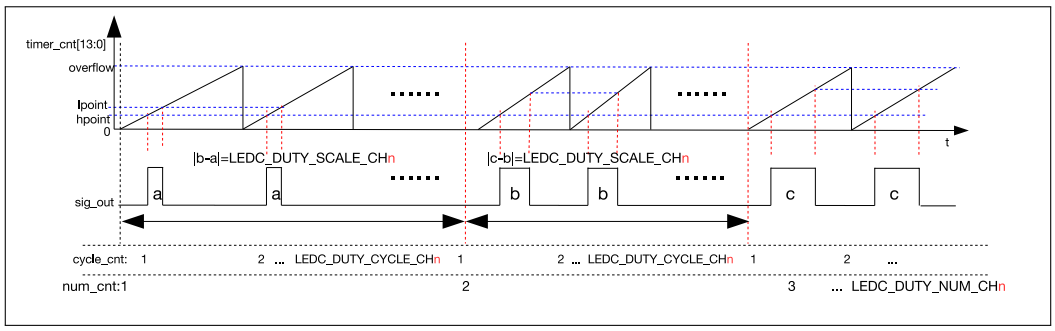
$$1023 + \frac{255}{256}$$

$$1023 + \frac{255}{256}$$

-
-



-
-


timer_cnt[13:0]
overflow
lpoint
hpoint
0
t
|b-a|=LEDC_DUTY_SCALE_CHn
|c-b|=LEDC_DUTY_SCALE_CHn
sig_out
a
a
b
b
c
c
cycle_cnt: 1 2 ... LEDC_DUTY_CYCLE_CHn 1 2 ... LEDC_DUTY_CYCLE_CHn 1 2 ...
num_cnt:1 2 3 ... LEDC_DUTY_NUM_CHn

-
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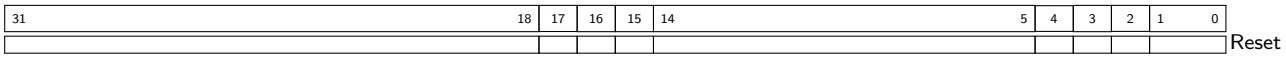
-


31
18
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16
15
14
5
4
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2
1
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Reset

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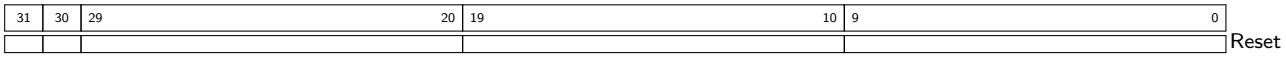
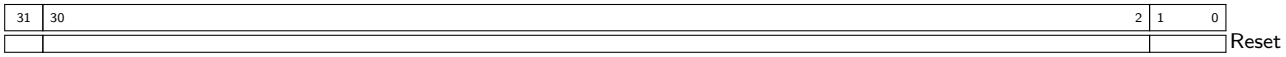
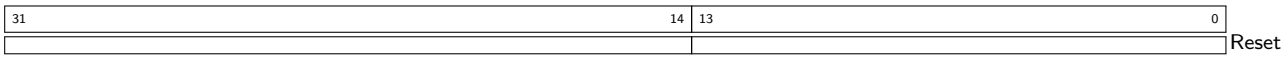
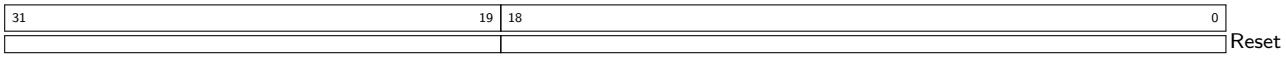
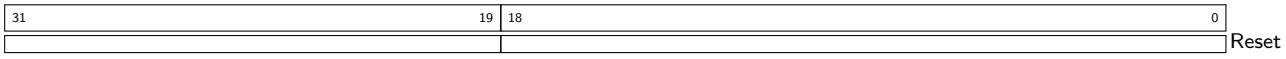
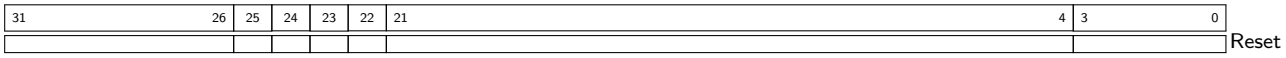

31
30
29
20
19
10
9
0
Reset


31
30
2
1
0
Reset


31
14
13
0
Reset


31
19
18
0
Reset


31
19
18
0
Reset


31
26
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23
22
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4
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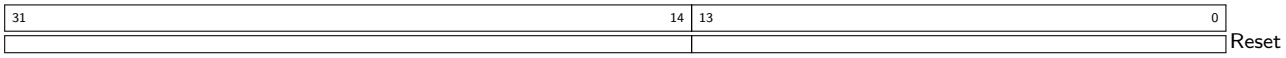
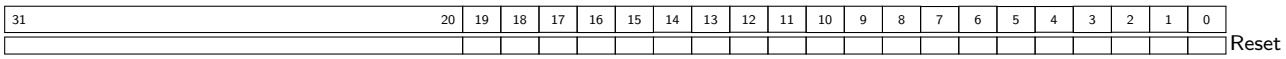
Reset


31
14
13
0
Reset


31
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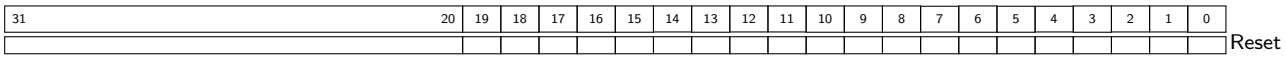
Reset


31
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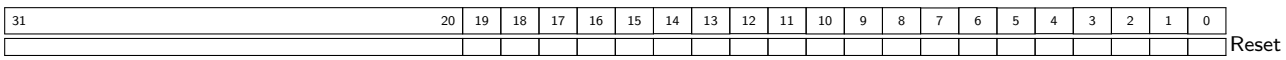
Reset


31
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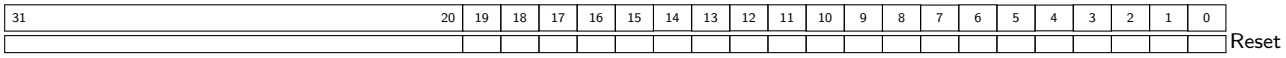
Reset


31
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11
10
9
8
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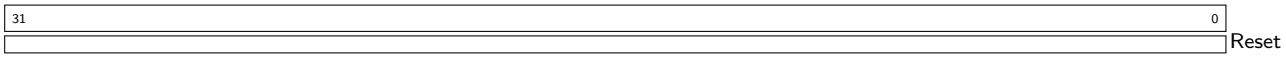
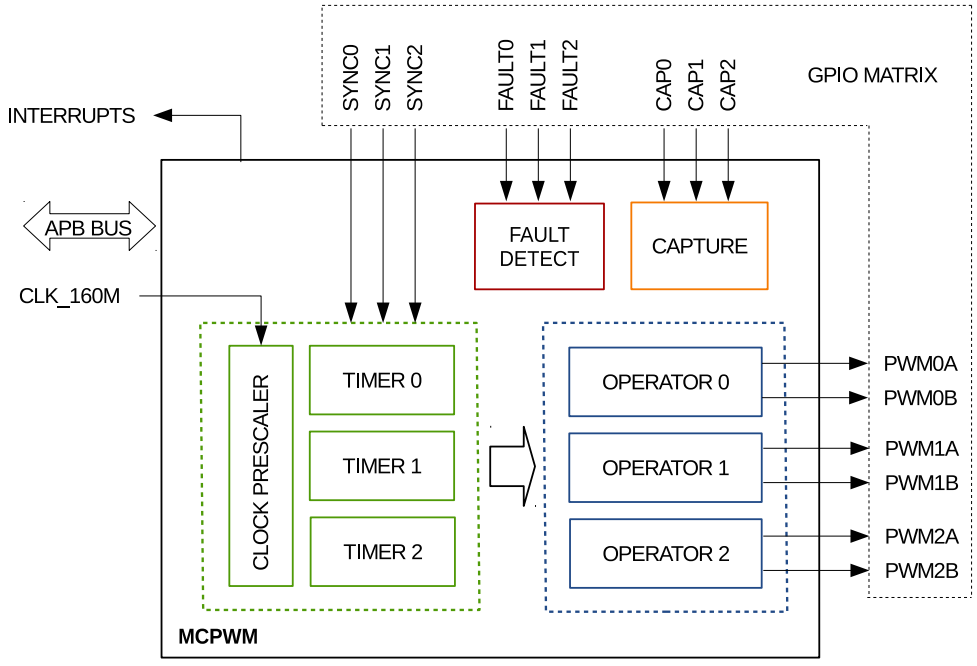
6
5
4
3
2
1
0
Reset


31
0
Reset


SYNC0
SYNC1
SYNC2
FAULT0
FAULT1
FAULT2
CAP0
CAP1
CAP2
GPIO MATRIX
INTERRUPTS
APB BUS
CLK_160M
FAULT DETECT
CAPTURE
CLOCK PRESCALER
TIMER 0
TIMER 1
TIMER 2
OPERATOR 0
OPERATOR 1
OPERATOR 2
PWM0A
PWM0B
PWM1A
PWM1B
PWM2A
PWM2B
MCPWM

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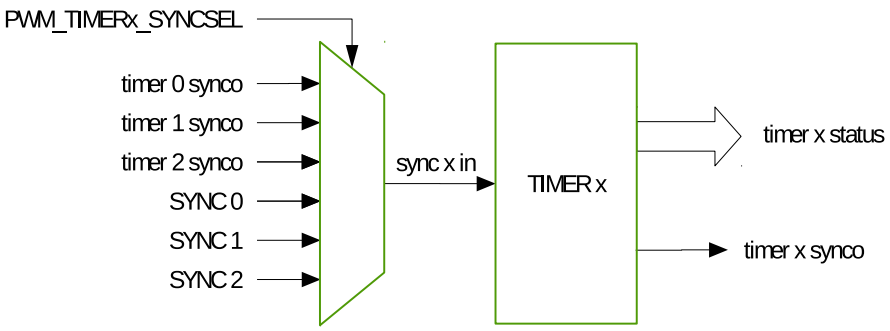
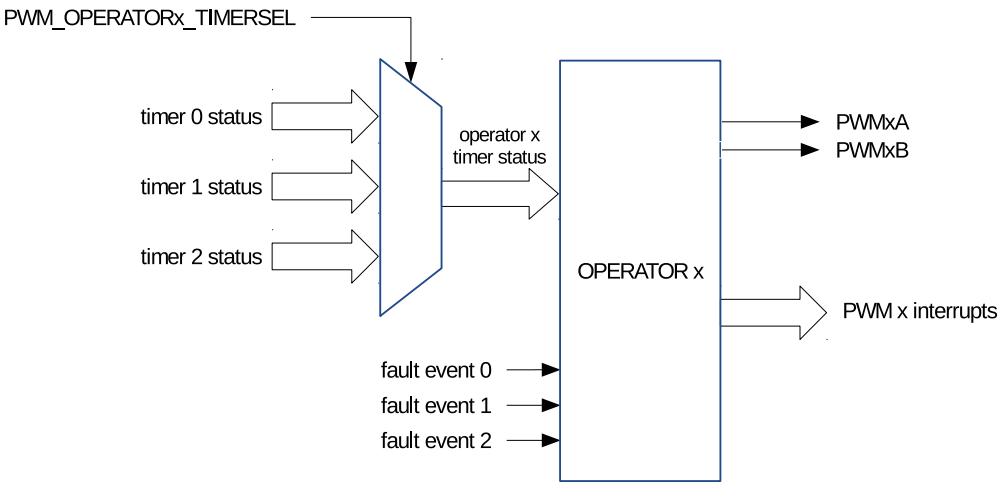
-

CRYPTO_PWM_CLK
CLOCK
PRESCALER
PWM_CLK


PWM_TIMERx_SYNCSEL
timer 0 synco
timer 1 synco
timer 2 synco
SYNC 0
SYNC 1
SYNC 2
sync x in
TIMER x
timer x status
timer x synco

-
-



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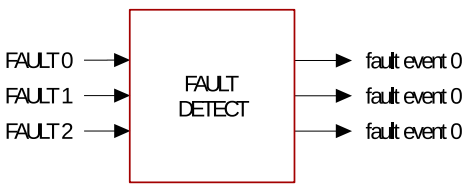

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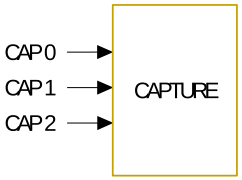
CAP0
CAP1
CAP2
CAPTURE

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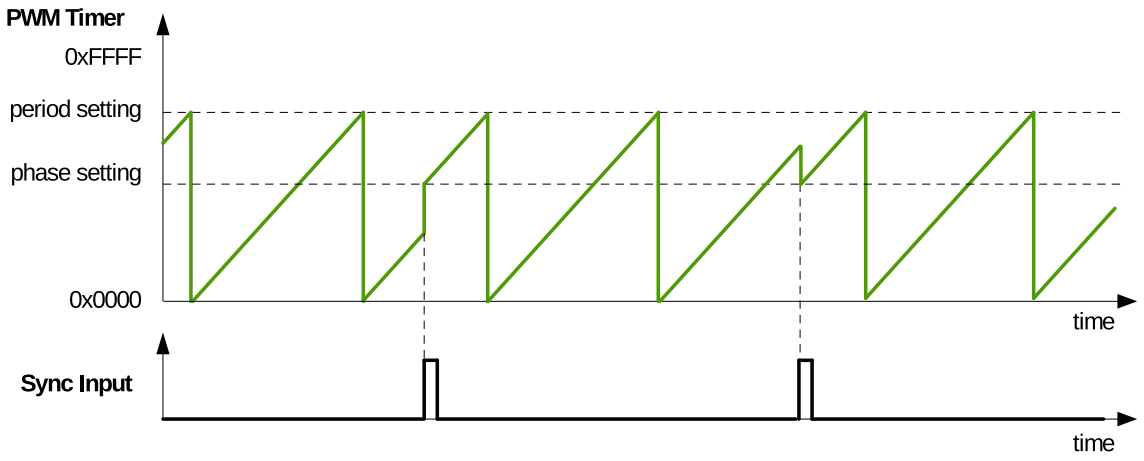
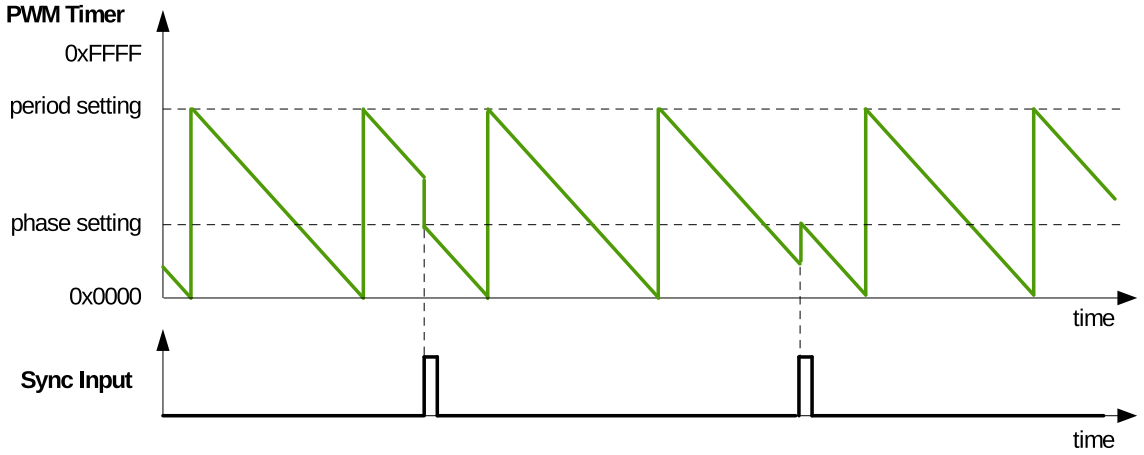
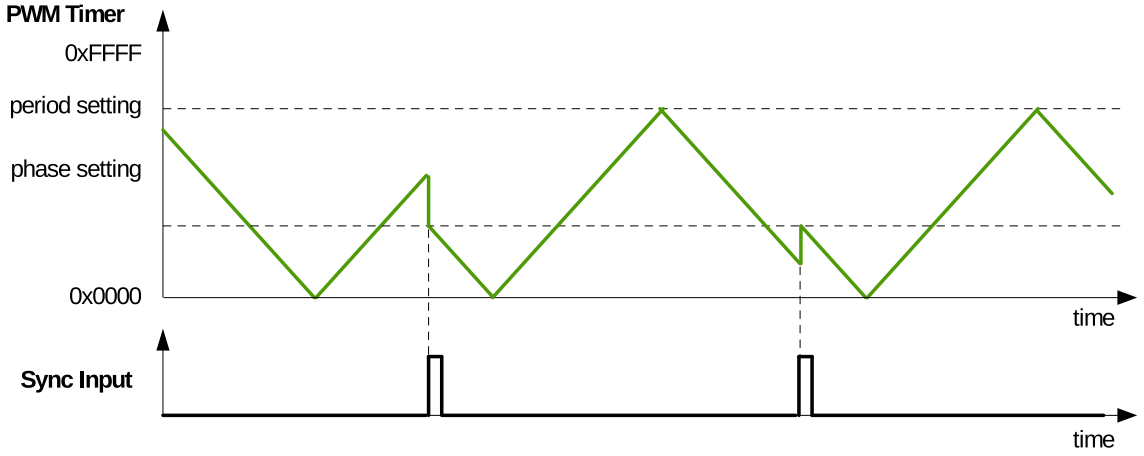
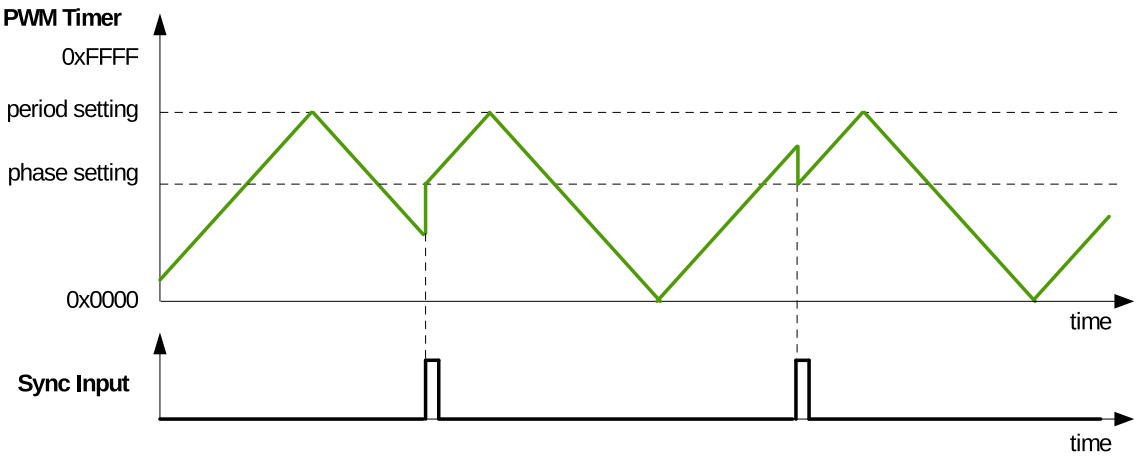

PWM Timer
0xFFFF
period setting
phase setting
0x0000
time
Sync Input
time


PWM Timer
0xFFFF
period setting
phase setting
0x0000
time
Sync Input
time


PWM Timer
0xFFFF
period setting
phase setting
0x0000
time
Sync Input
time


PWM Timer
0xFFFF
period setting
phase setting
0x0000
time
Sync Input
time

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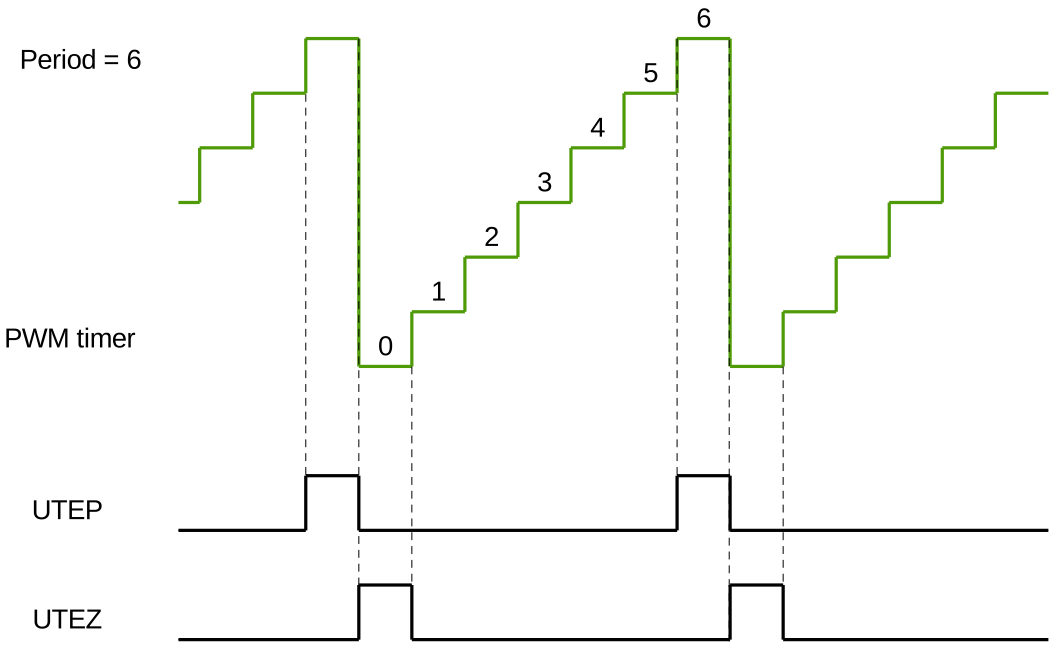
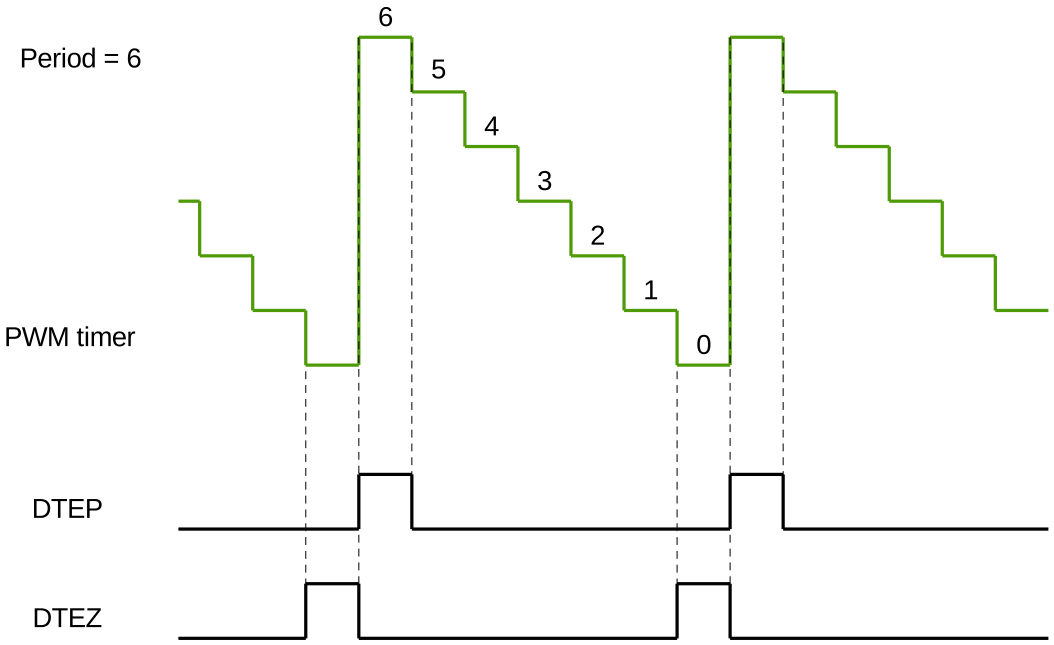
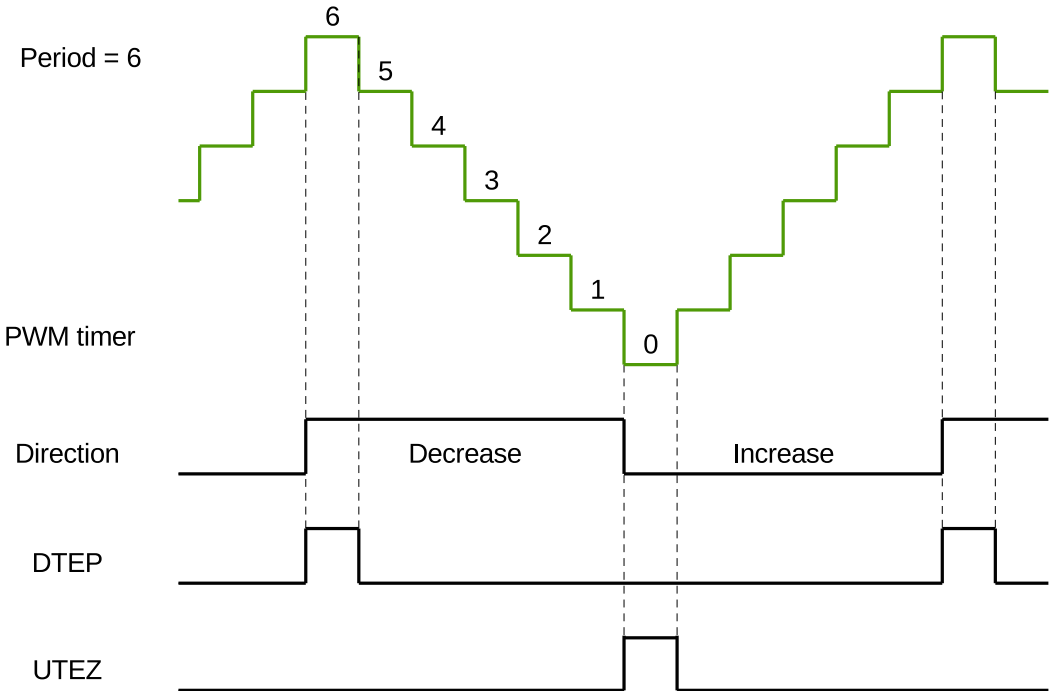
-

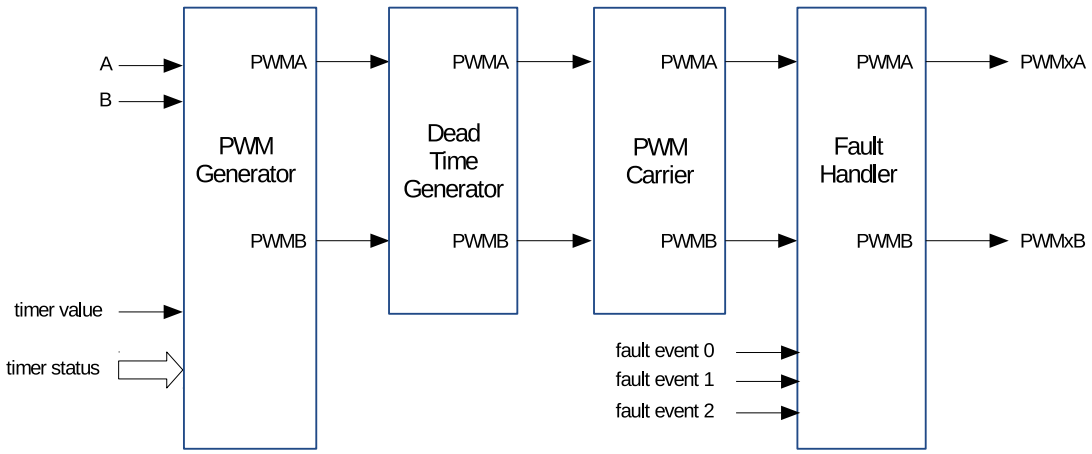

Period = 6
PWM timer
0
1
2
3
4
5
6
UTEP
UTEZ


Period = 6
6
5
4
3
2
1
0
PWM timer
DTEP
DTEZ


Period = 6
6
5
4
3
2
1
0
PWM timer
Direction
Decrease
Increase
DTEP
UTEZ

-
-

-
-
-
-


A
B
timer value
timer status
PWM Generator
PWMA
PWMB
Dead Time Generator
PWMA
PWMB
PWM Carrier
PWMA
PWMB
Fault Handler
PWMA
PWMB
fault event 0
fault event 1
fault event 2
PWMxA
PWMxB

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-
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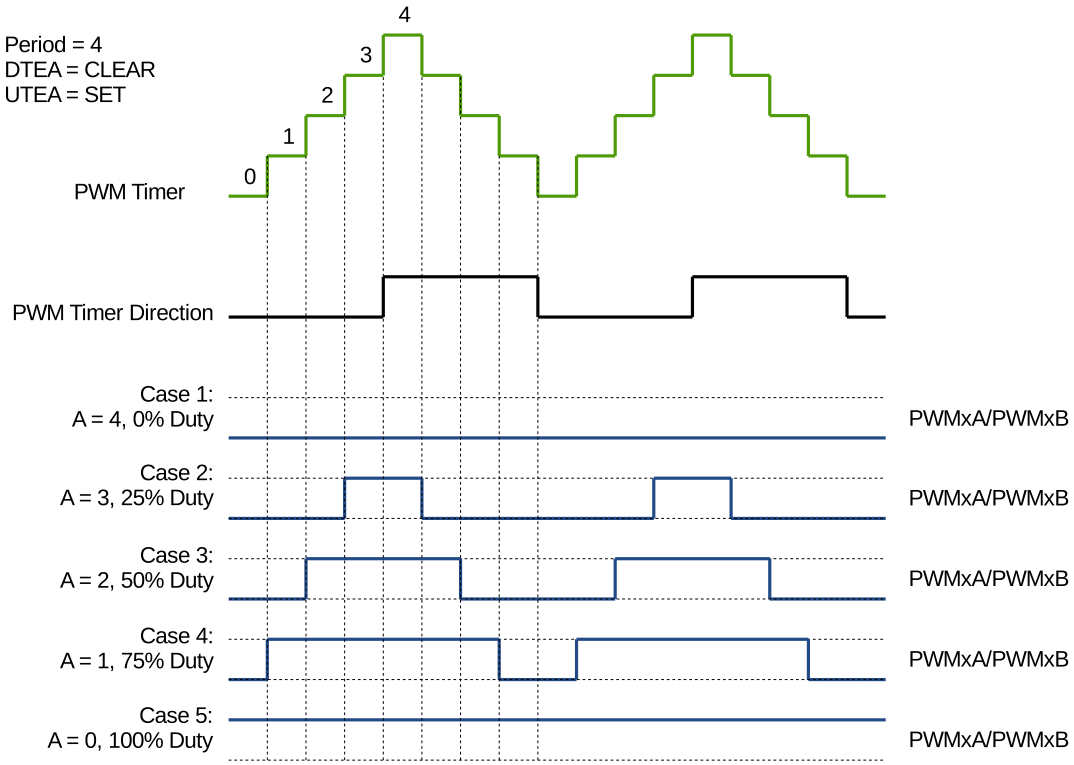
$$Duty = (Period - A) \div Period$$



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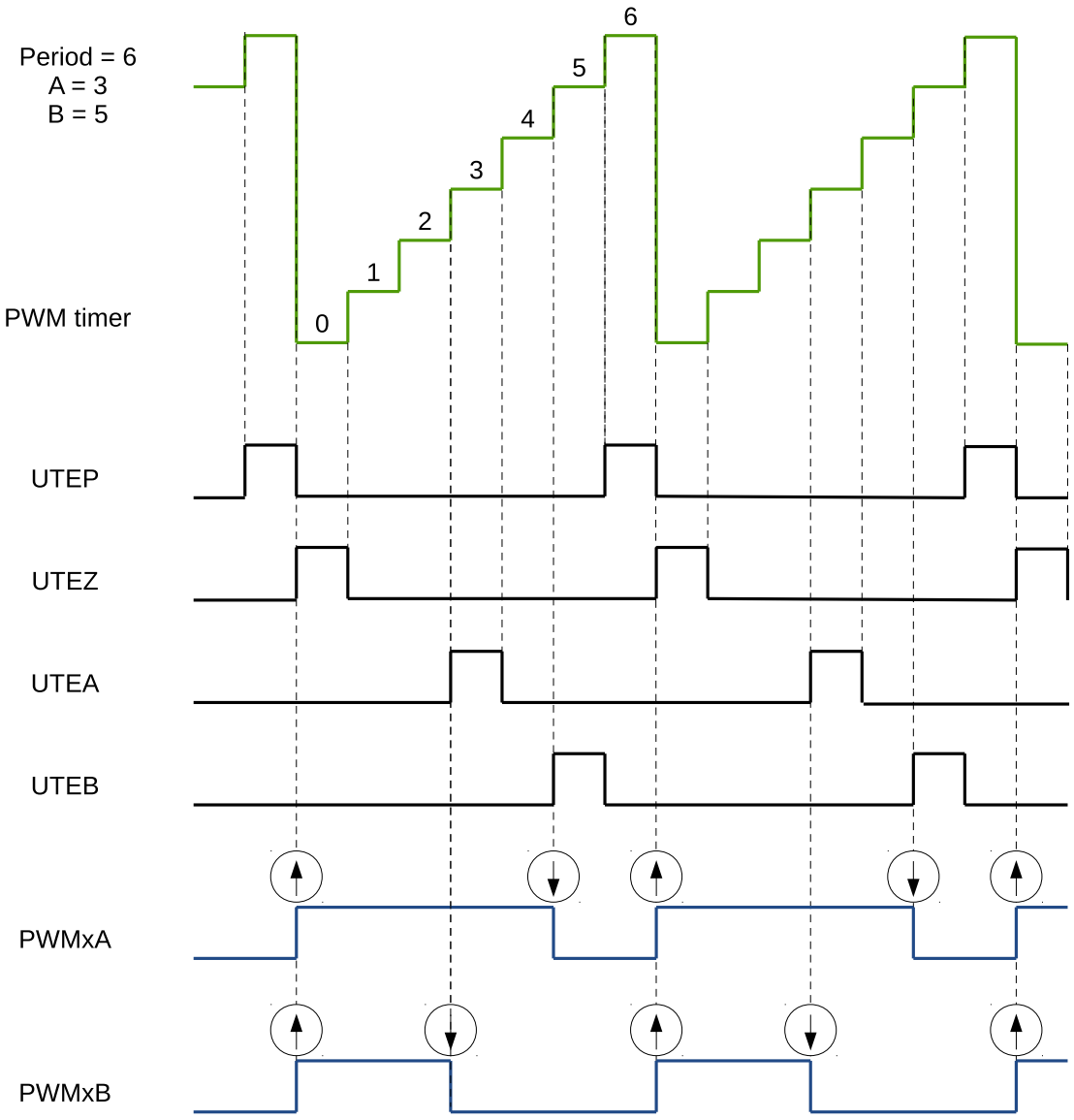
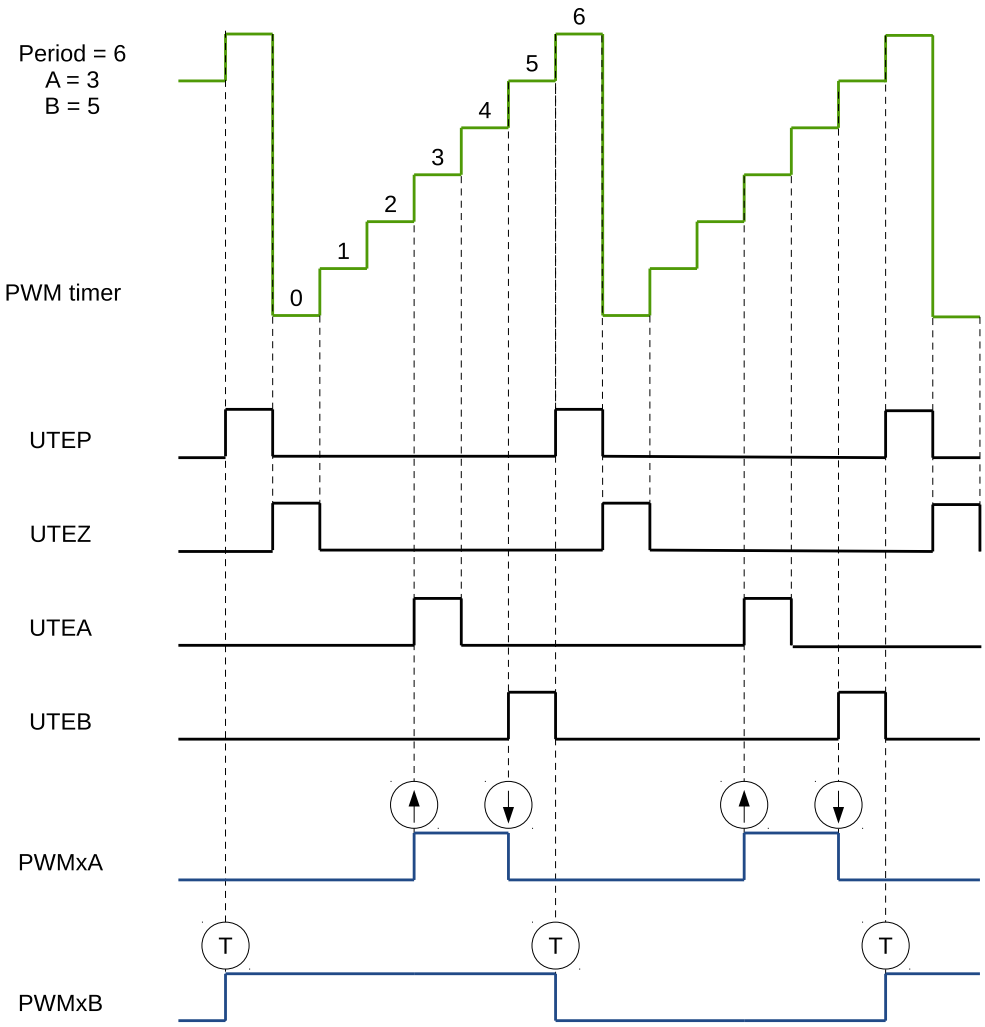
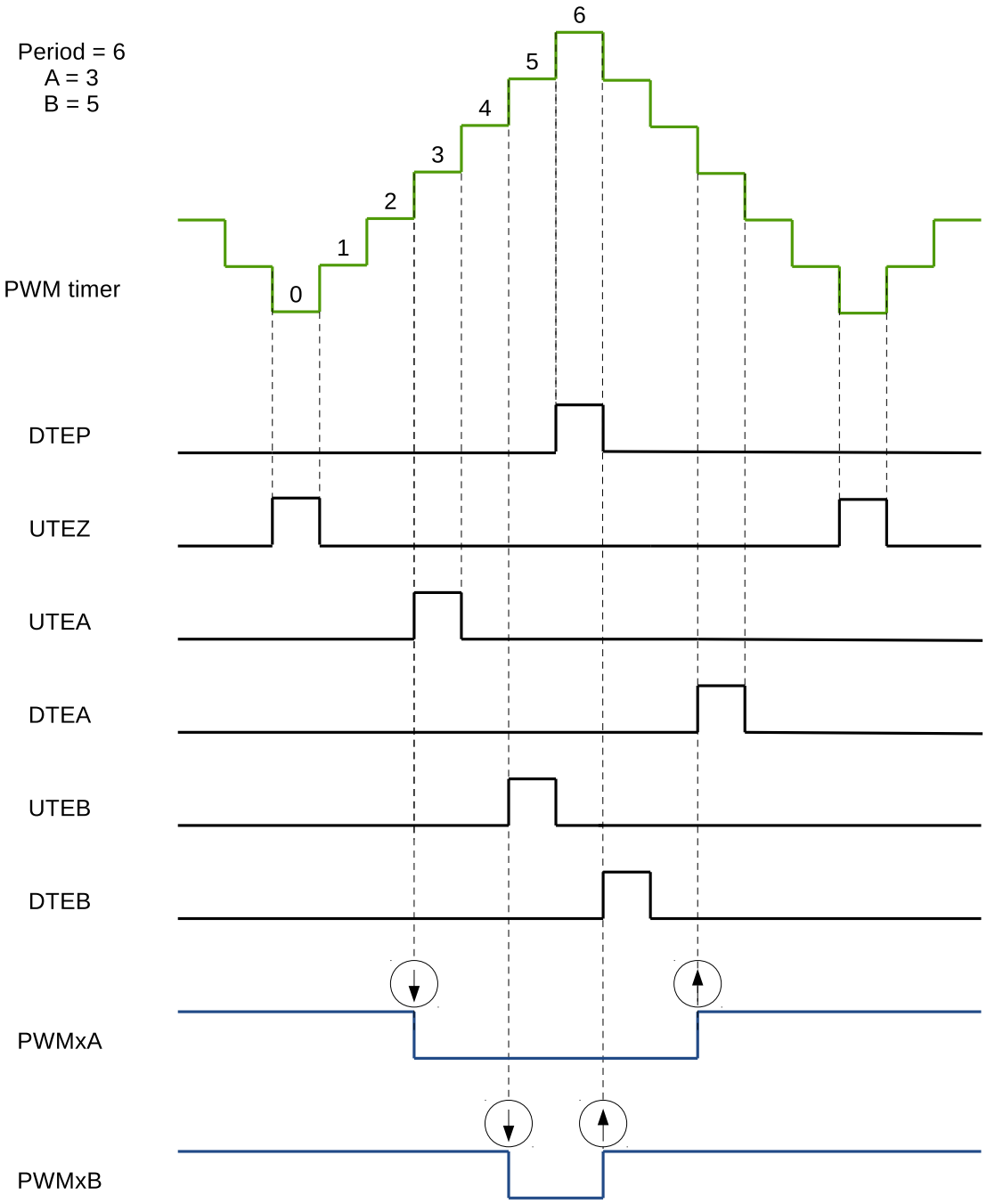


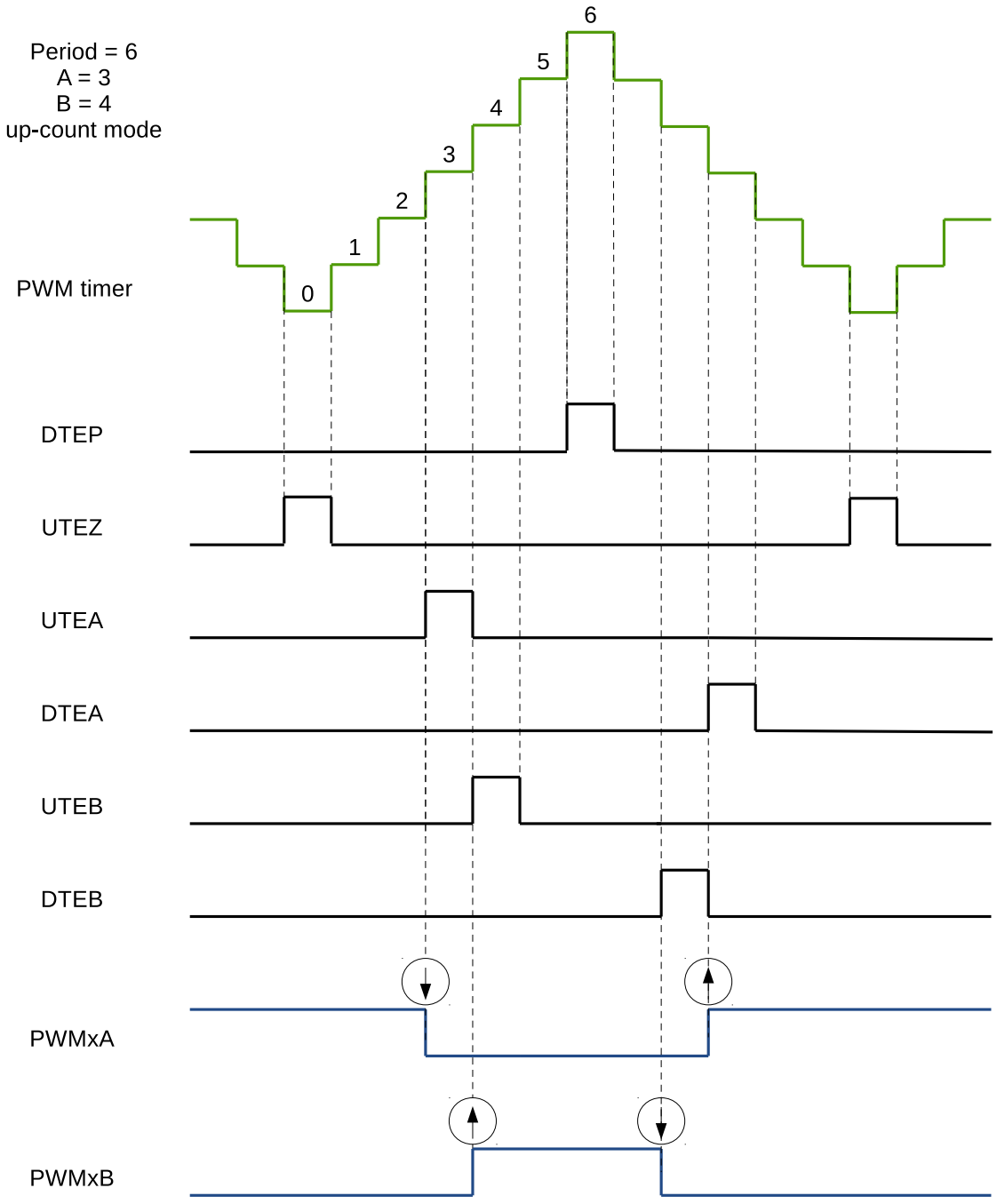
$$Period = (MCPWMTIMERPERIOD + 1) \times T_{PTclk}$$



$$Period = (MCPWMTIMERPERIOD + 1) \times T_{PTclk}$$



$$Period = (2 \times MCPWMTIMERPERIOD) \times T_{PTclk}$$



$$Period = (2 \times MCPWMTIMERPERIOD) \times T_{PTclk}$$

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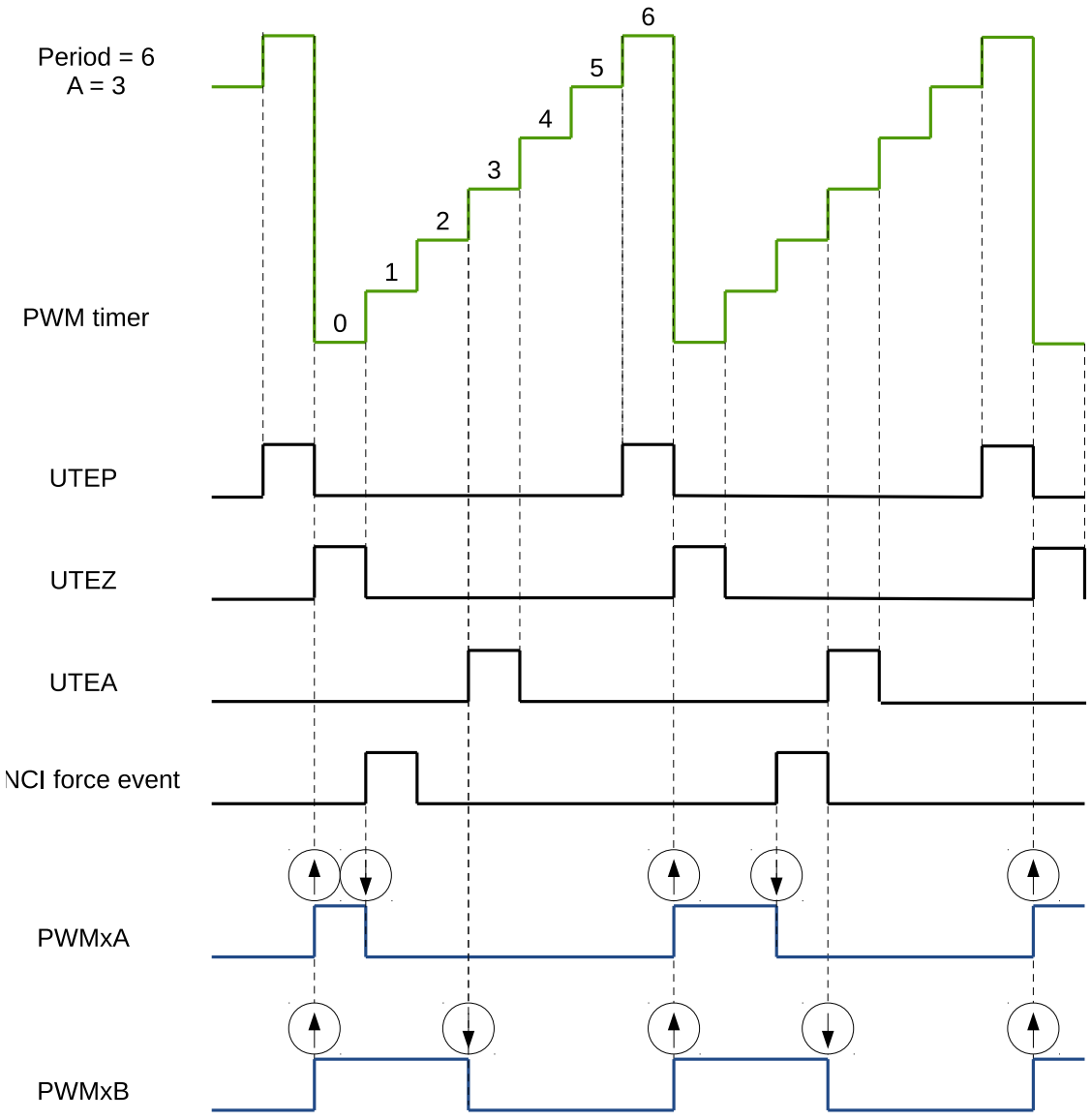
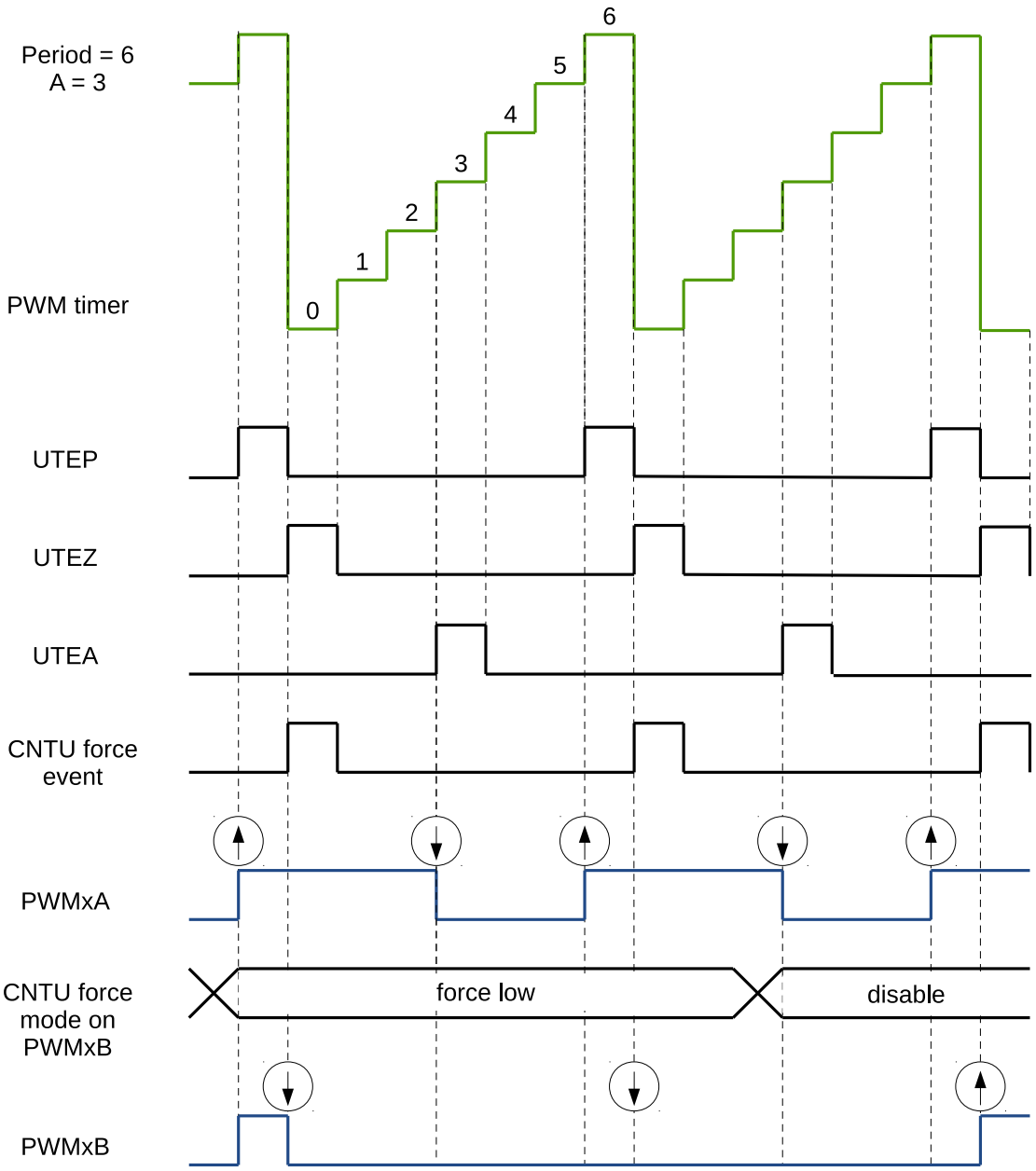

Period = 6
A = 3
PWM timer
0
1
2
3
4
5
6
UTEP
UTEZ
UTEA
NCI force event
PWMxA
PWMxB


Period = 6
A = 3
PWM timer
0
1
2
3
4
5
6
UTEP
UTEZ
UTEA
CNTU force event
PWMxA
CNTU force mode on PWMxB
force low
disable
PWMxB

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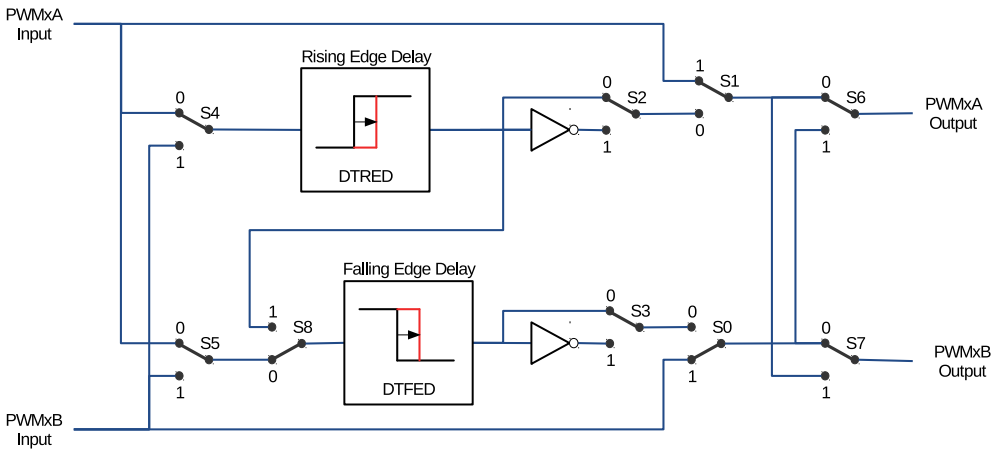
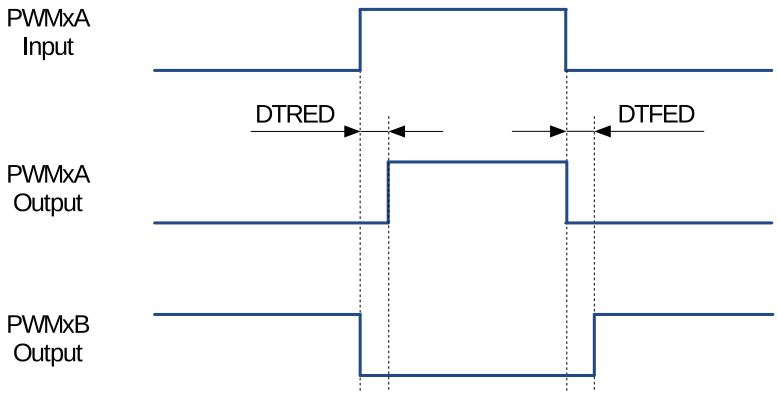
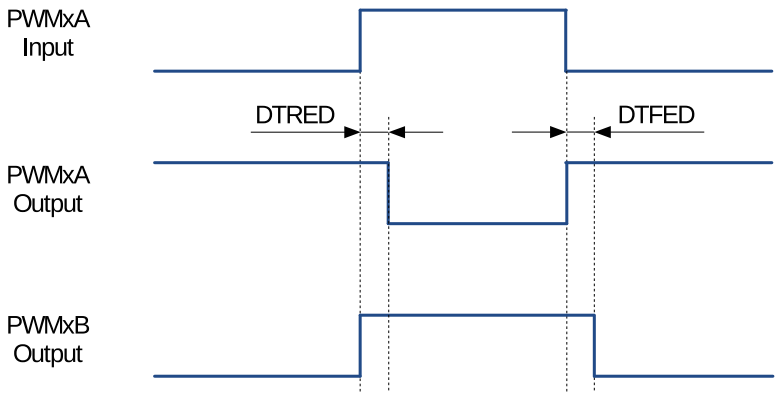
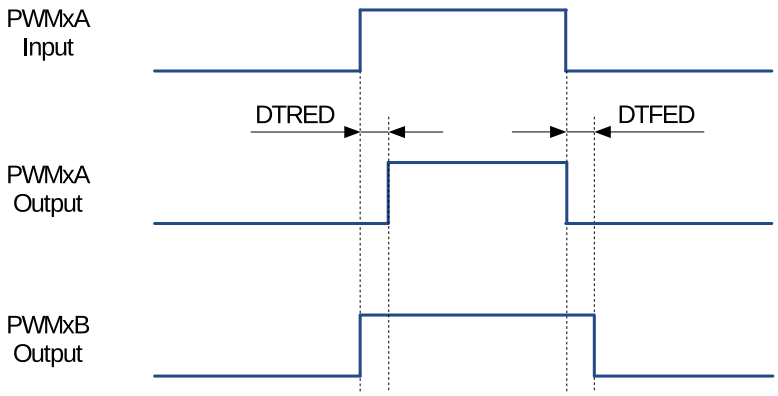
-
-
-

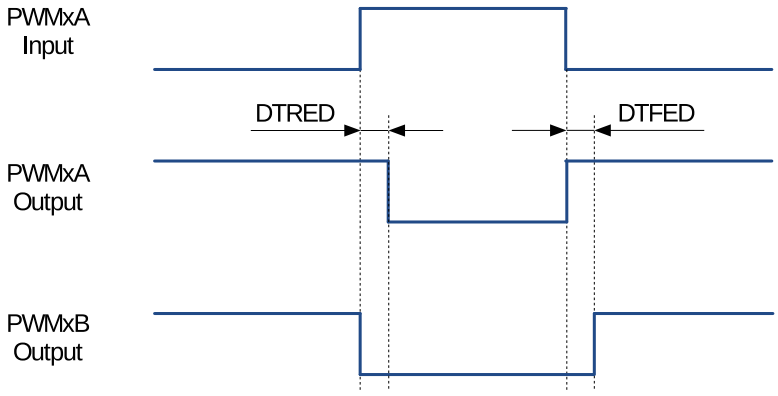

PWMxA
Input
Rising Edge Delay
DTRED
S4
S1
S2
S6
PWMxA
Output
Falling Edge Delay
DTFED
S5
S8
S3
S0
S7
PWMxB
Output
PWMxB
Input

-
-
-


PWMxA
Input
DTRED
DTFED
PWMxA
Output
PWMxB
Output


PWMxA
Input
DTRED
DTFED
PWMxA
Output
PWMxB
Output


PWMxA
Input
DTRED
DTFED
PWMxA
Output
PWMxB
Output


PWMxA
Input
DTRED
DTFED
PWMxA
Output
PWMxB
Output

$$FED = MCPWMDTFED \times T_{DTclk}$$

$$RED = MCPWMDTRED \times T_{DTclk}$$

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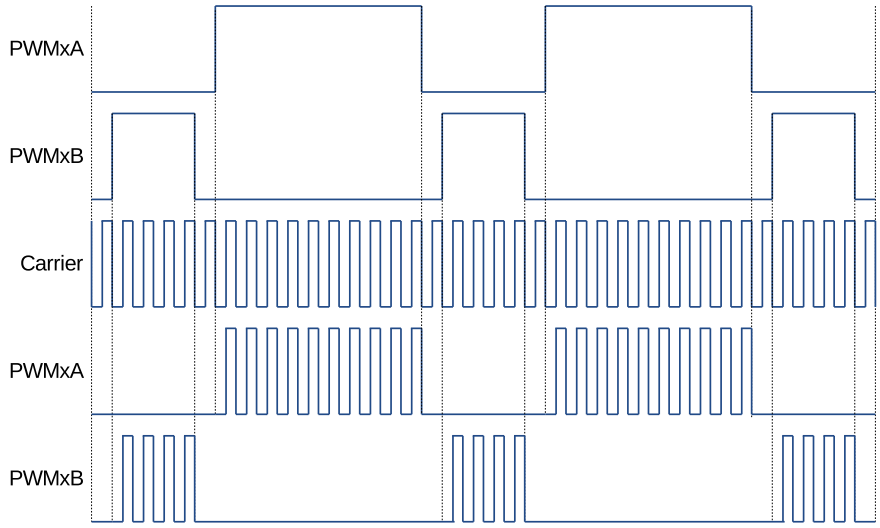
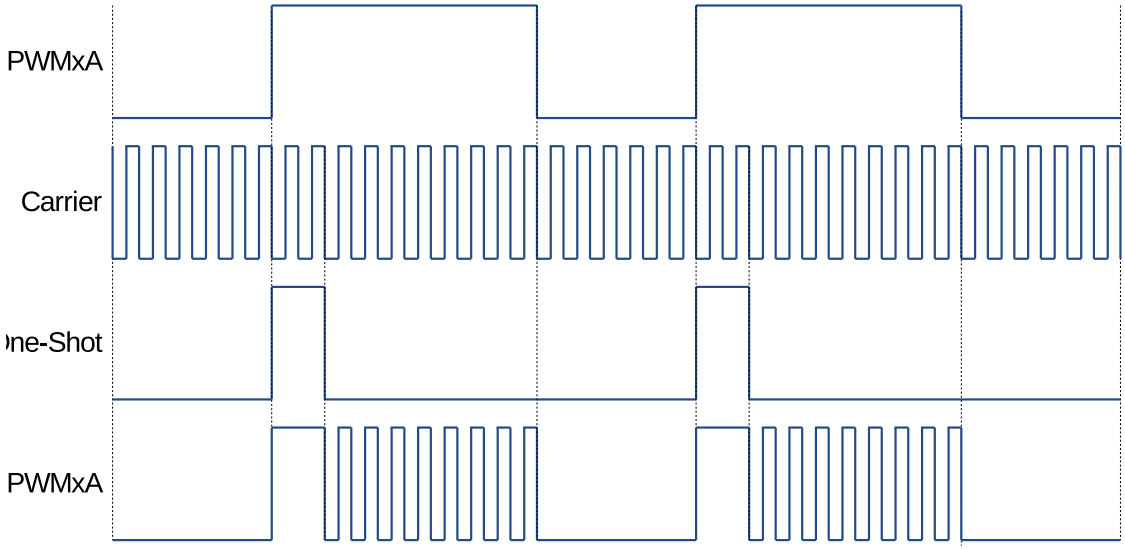


$$T_{1stpulse} = T_{PWMclk} \times 8 \times (MCPWMCARRIERPRESCALE + 1) \times (MCPWMCARRIEROSHTWTH + 1)$$

- T_{PMWclk}
- $(MCPWMCARRIEROSHTWTH + 1)$

- $(MCPWMCARRIERPRESCALE + 1)$



$$Duty = MCPWMCARRIERDUTY \div 8$$

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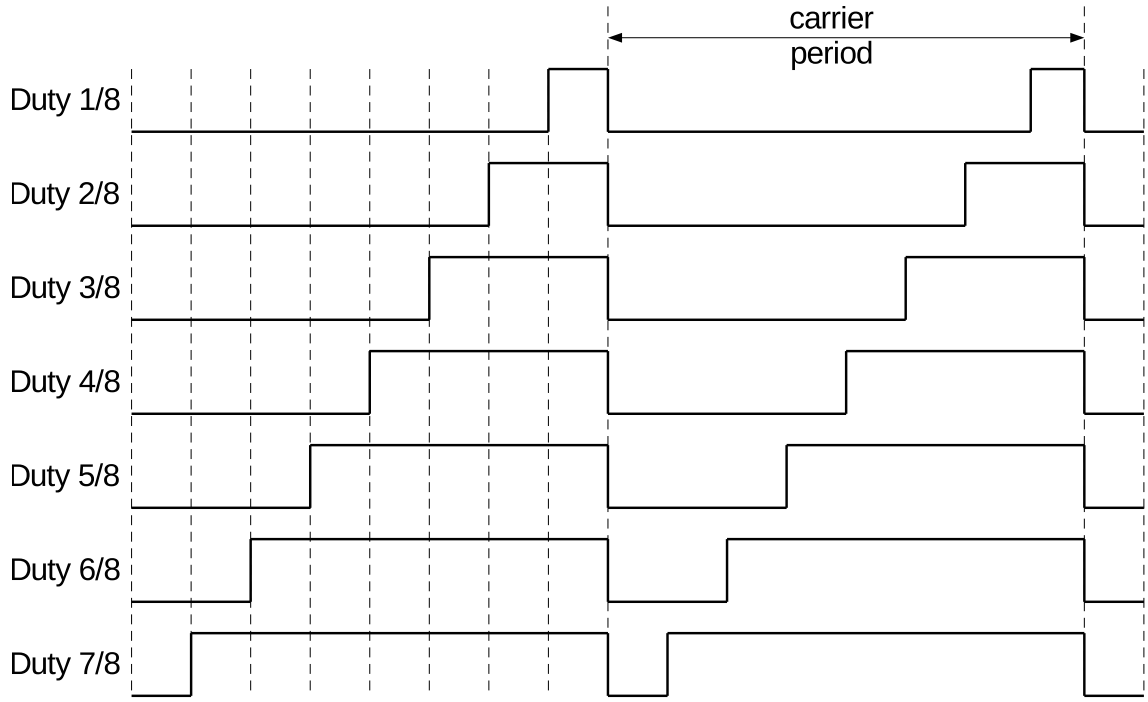
carrier
period
Duty 1/8
Duty 2/8
Duty 3/8
Duty 4/8
Duty 5/8
Duty 6/8
Duty 7/8

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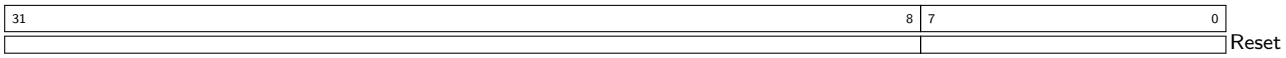
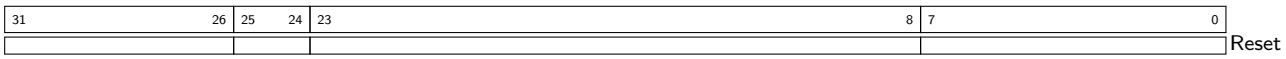
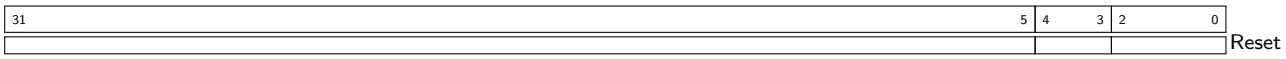

31
8
7
0
Reset


31
26
25
24
23
8
7
0
Reset


31
5
4
3
2
0
Reset

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-
-
-
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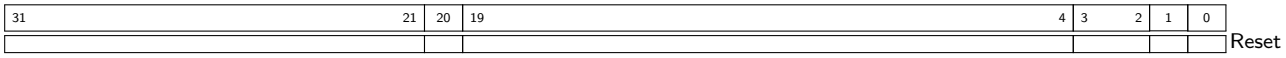
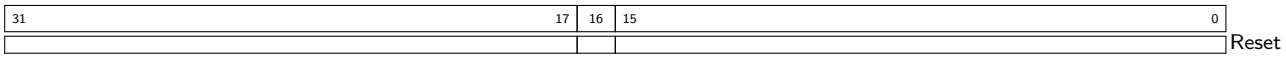
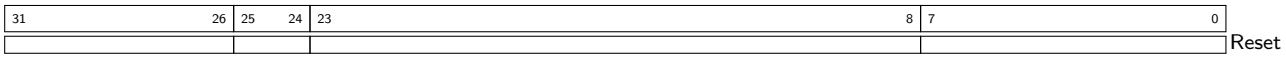
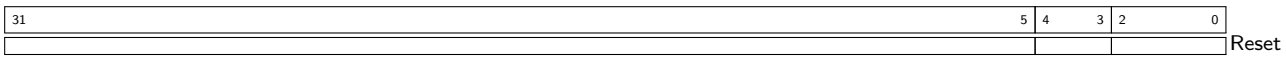
-
-
-


31
21
20
19
4
3
2
1
0
Reset


31
17
16
15
0
Reset


31
26
25
24
23
8
7
0
Reset


31
5
4
3
2
0
Reset

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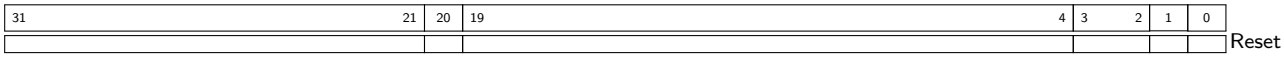
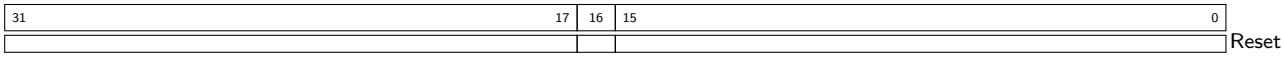
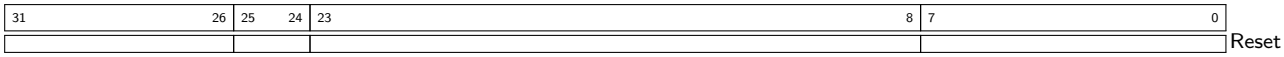
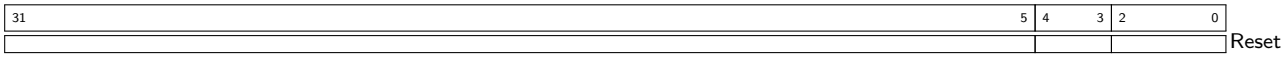

31
21
20
19
4
3
2
1
0
Reset


31
17
16
15
0
Reset


31
26
25
24
23
8
7
0
Reset


31
5
4
3
2
0
Reset

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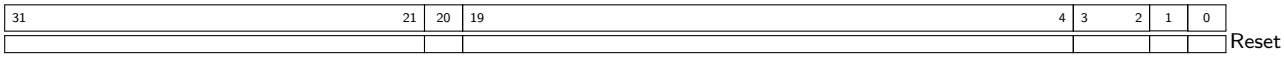
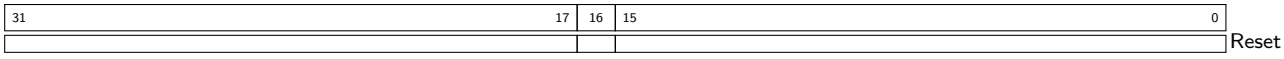
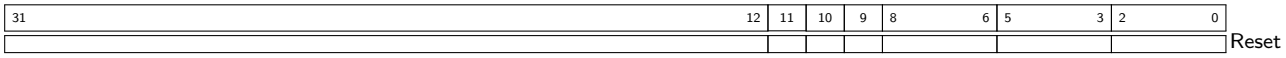

31
21
20
19
4
3
2
1
0
Reset


31
17
16
15
0
Reset


31
12
11
10
9
8
6
5
3
2
0
Reset

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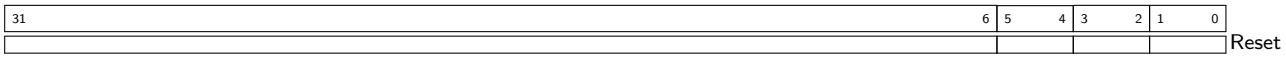
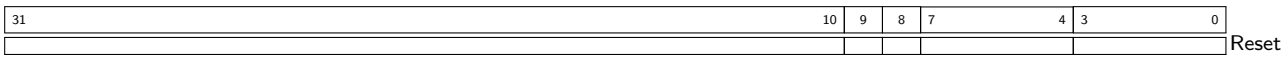
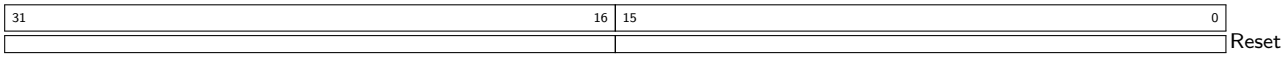
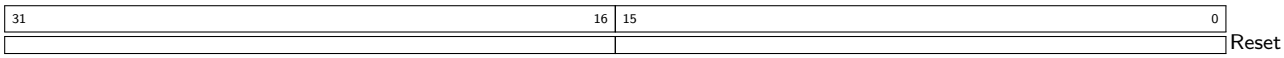
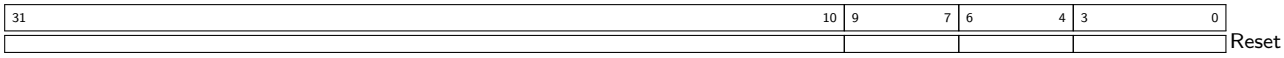
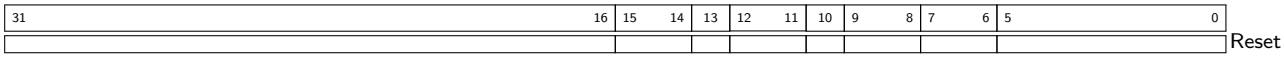

31
6
5
4
3
2
1
0
Reset

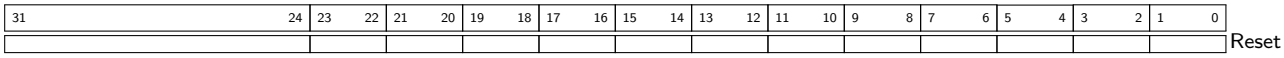

31
10
9
8
7
4
3
0
Reset

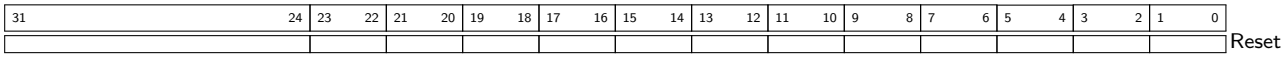

31
16
15
0
Reset


31
16
15
0
Reset


31
10
9
7
6
4
3
0
Reset


31
16
15
14
13
12
11
10
9
8
7
6
5
0
Reset


31 24
23 22
21 20
19 18
17 16
15 14
13 12
11 10
9 8
7 6
5 4
3 2
1 0
Reset


31 24
23 22
21 20
19 18
17 16
15 14
13 12
11 10
9 8
7 6
5 4
3 2
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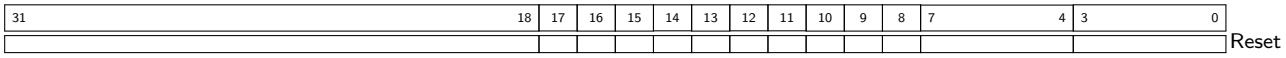
Reset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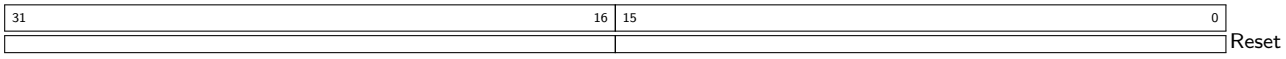
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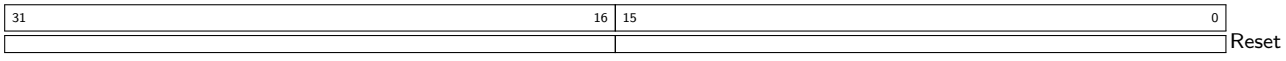
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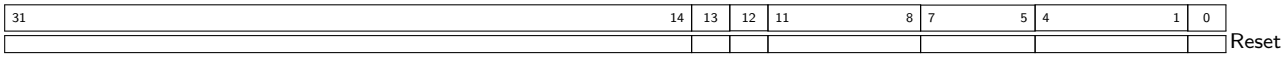
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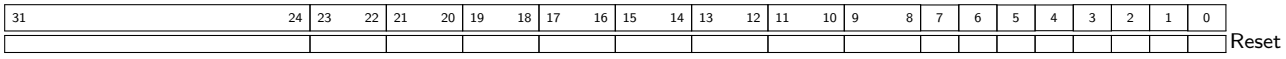
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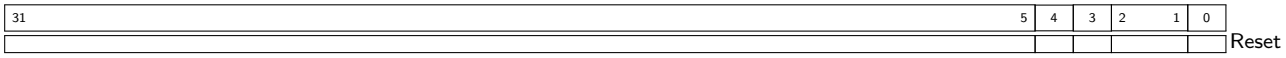
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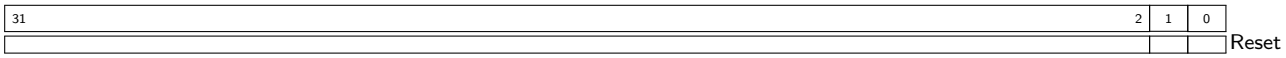
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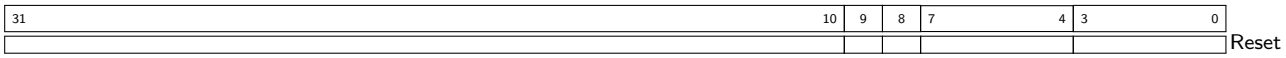
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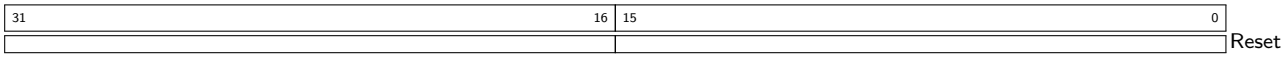
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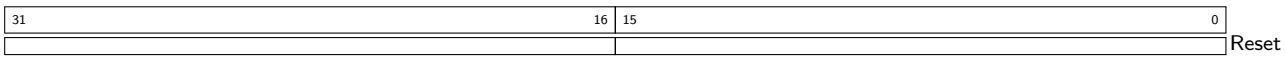
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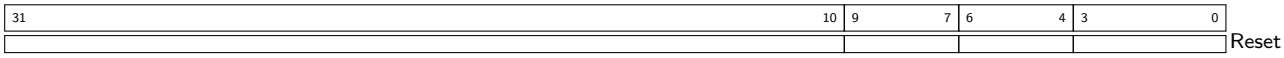
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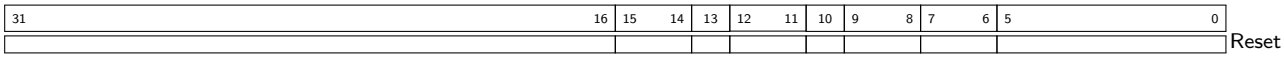
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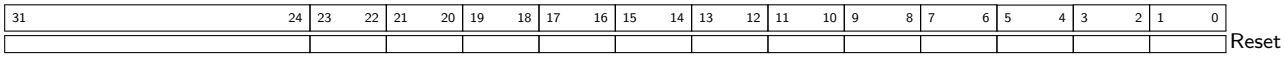
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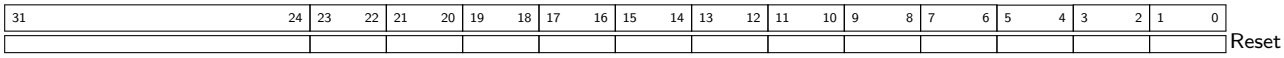
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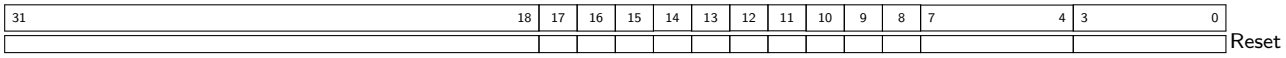
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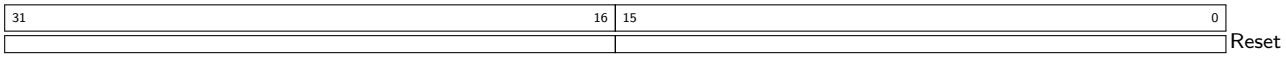
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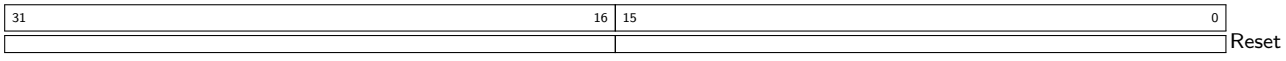
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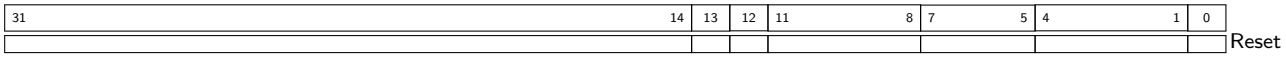
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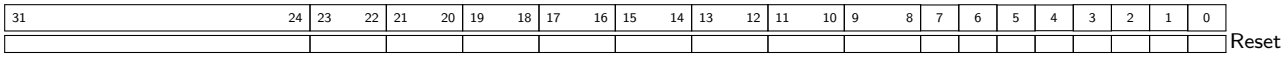
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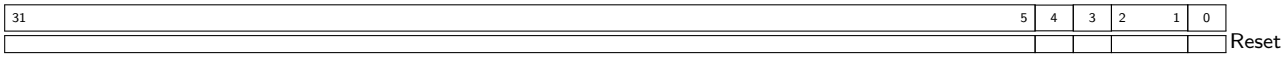
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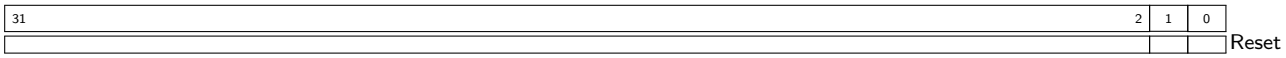
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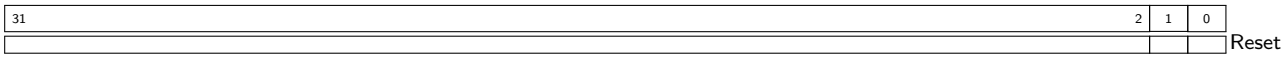
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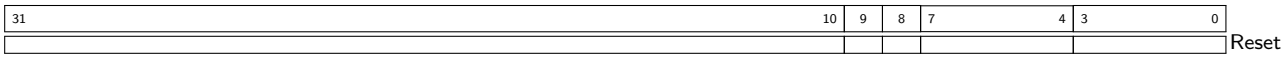
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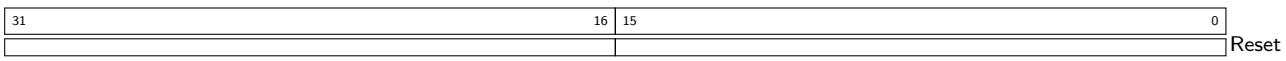
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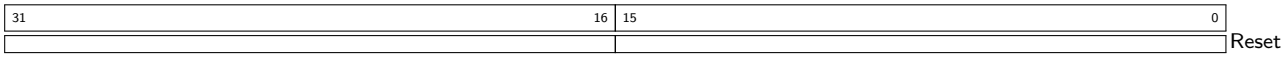
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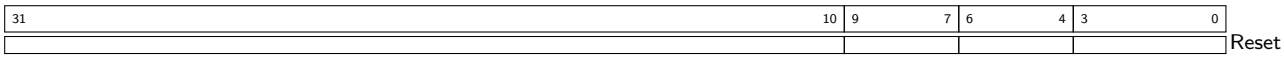
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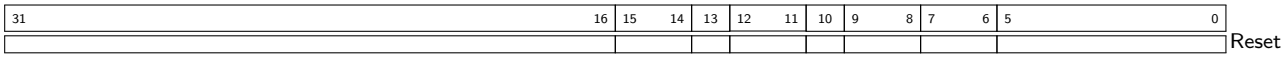
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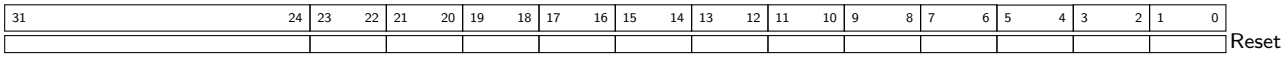
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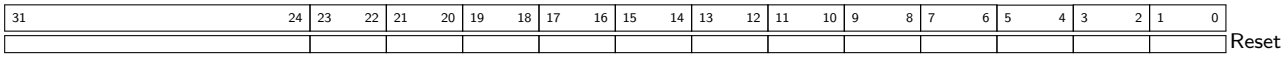
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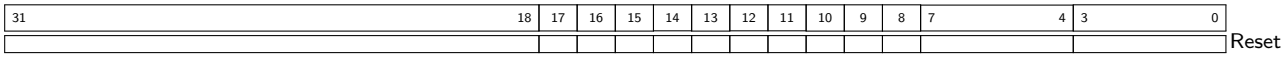
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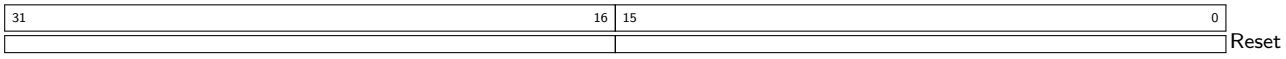
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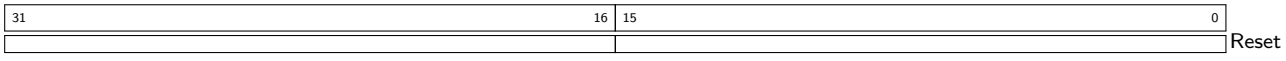
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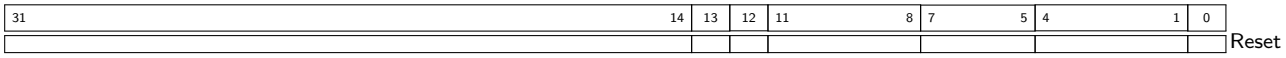
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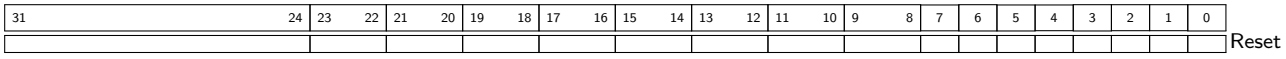
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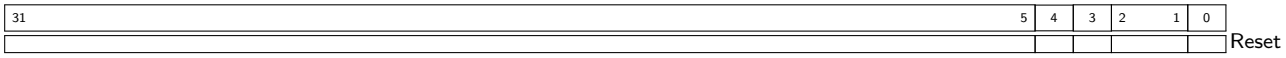
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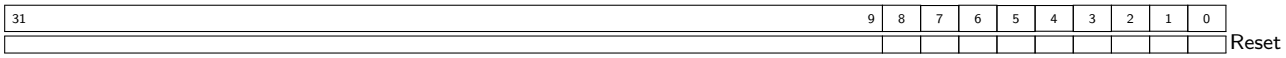
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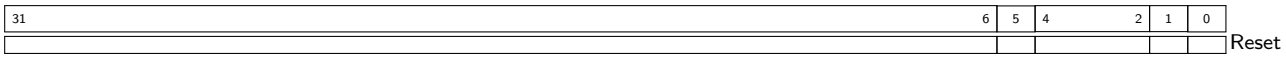
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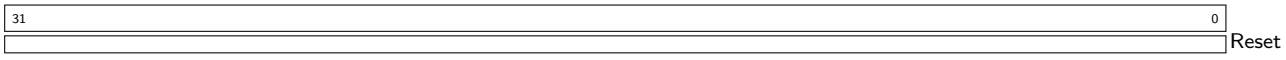
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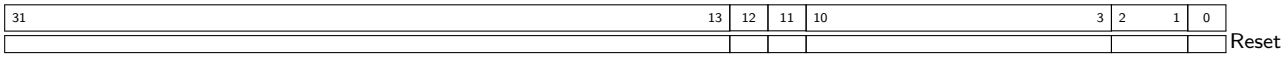
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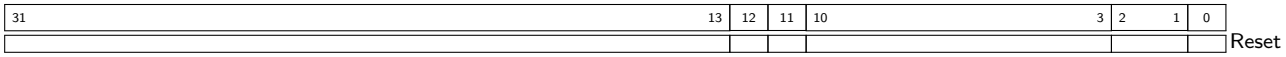
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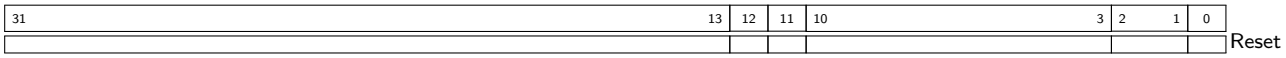
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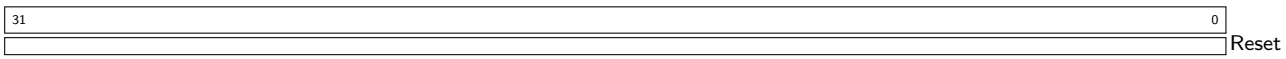
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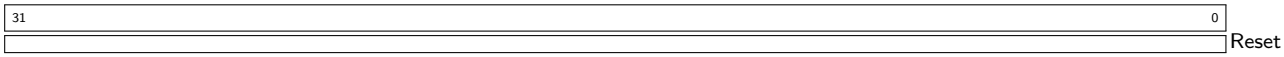
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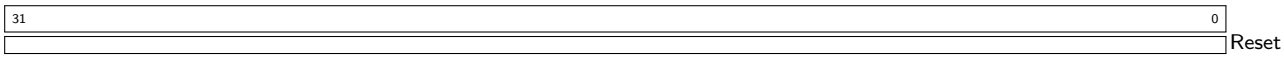
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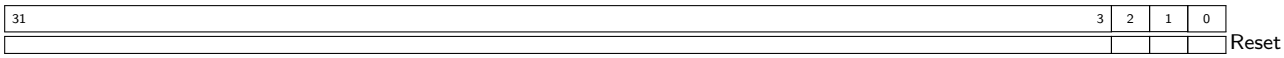
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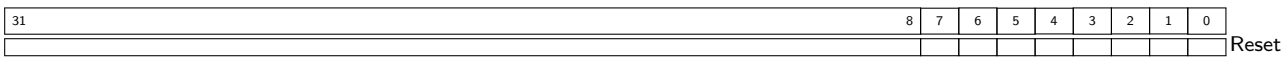
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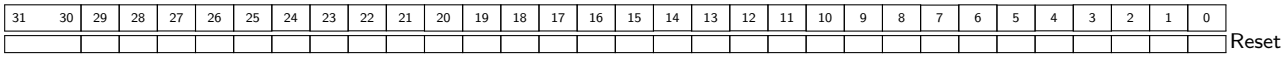
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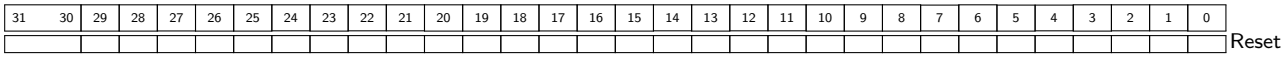
31 30
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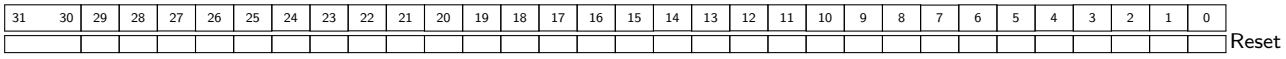
Reset


31 30
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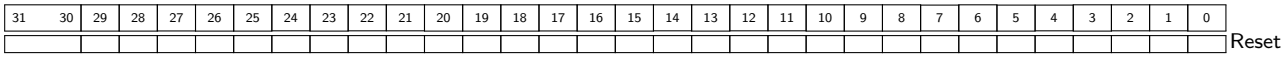
Reset


31 30
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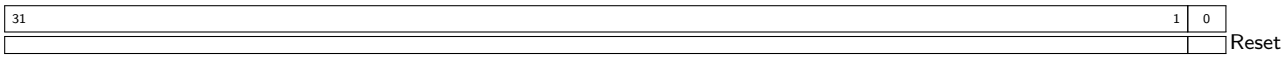
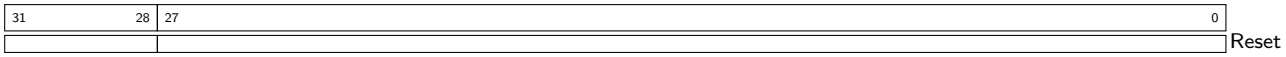
Reset


31
1
0
Reset


31
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27
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Reset

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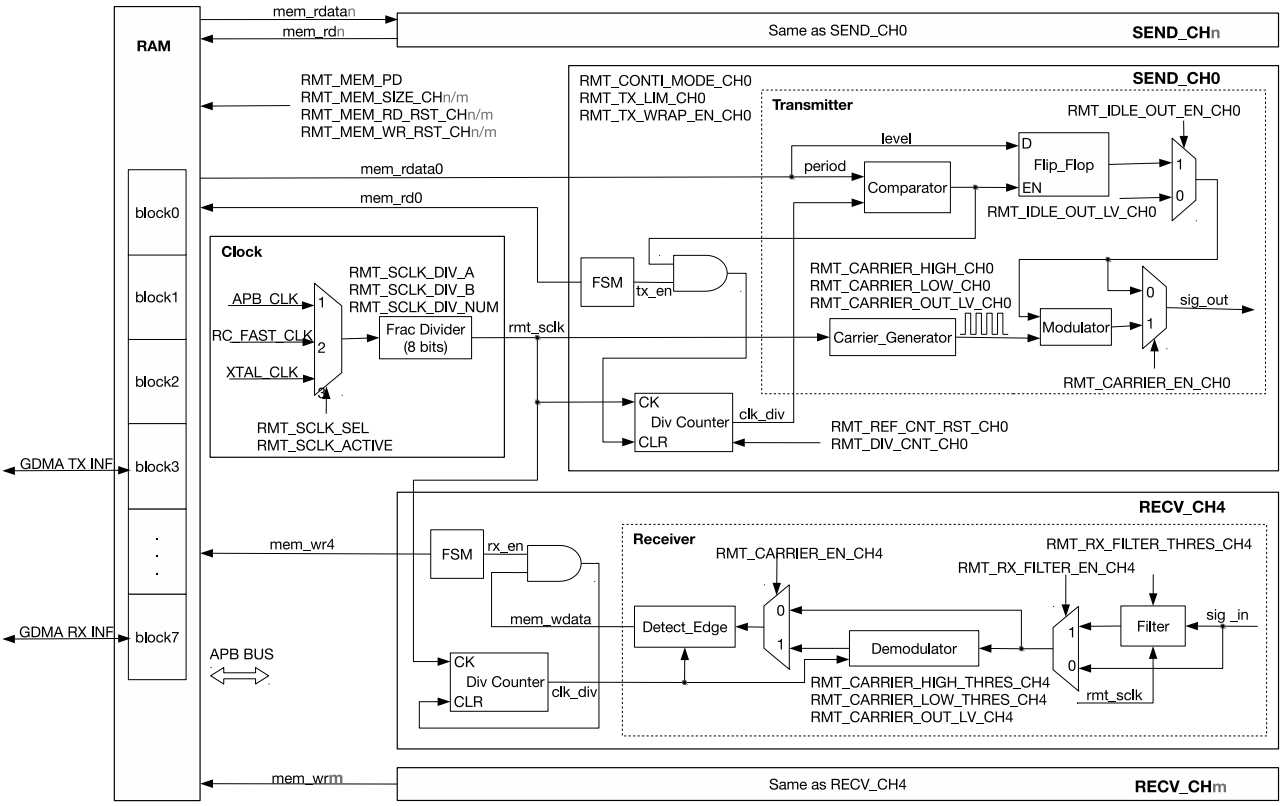
RAM
mem_rdatan
mem_rdn
Same as SEND_CH0
SEND_CHn
RMT_MEM_PD
RMT_MEM_SIZE_CHn/m
RMT_MEM_RD_RST_CHn/m
RMT_MEM_WR_RST_CHn/m
RMT_CONTI_MODE_CH0
RMT_TX_LIM_CH0
RMT_TX_WRAP_EN_CH0
SEND_CH0
Transmitter
RMT_IDLE_OUT_EN_CH0
level
period
Comparator
D
Flip_Flop
EN
RMT_IDLE_OUT_LV_CH0
mem_rdata0
mem_rd0
block0
block1
block2
block3
block7
GDMA TX INF
GDMA RX INF
Clock
APB_CLK
RC_FAST_CLK
XTAL_CLK
RMT_SCLK_DIV_A
RMT_SCLK_DIV_B
RMT_SCLK_DIV_NUM
Frac Divider
(8 bits)
RMT_SCLK_SEL
RMT_SCLK_ACTIVE
rmt_sclk
FSM
tx_en
RMT_CARRIER_HIGH_CH0
RMT_CARRIER_LOW_CH0
RMT_CARRIER_OUT_LV_CH0
Carrier_Generator
Modulator
sig_out
RMT_CARRIER_EN_CH0
CK
Div Counter
CLR
clk_div
RMT_REF_CNT_RST_CH0
RMT_DIV_CNT_CH0
RECV_CH4
Receiver
mem_wr4
FSM
rx_en
mem_wdata
RMT_CARRIER_EN_CH4
RMT_RX_FILTER_THRES_CH4
RMT_RX_FILTER_EN_CH4
Detect_Edge
Demodulator
Filter
sig_in
rmt_sclk
RMT_CARRIER_HIGH_THRES_CH4
RMT_CARRIER_LOW_THRES_CH4
RMT_CARRIER_OUT_LV_CH4
APB BUS
mem_wrm
Same as RECV_CH4
RECV_CHm

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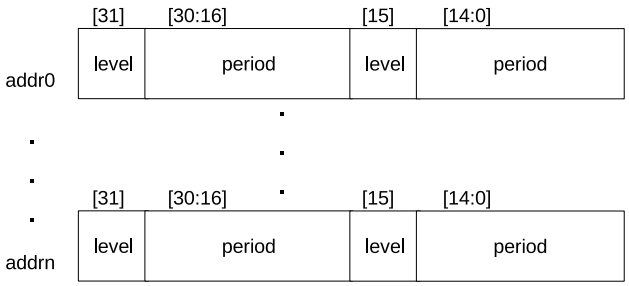

$$3 \times T_{apbclk} + 5 \times T_{rmtsclk} < period \times T_{clkdiv} (1)$$

$period \times T_{clkdiv}$

- $(3 \times T_{apbclk} + 5 \times T_{rmtsclk})$
- $\times T_{clkdiv} (2^{15} - 1) \times T_{rmtsclk} \times$

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$$RMTSCLKDIVNUM + 1 + RMTSCLKDIVA/RMTSCLKDIVB$$

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$$6 \times T_{apbclk} + 12 \times T_{rmtsclk} < period \times T_{clkdiv} (2)$$

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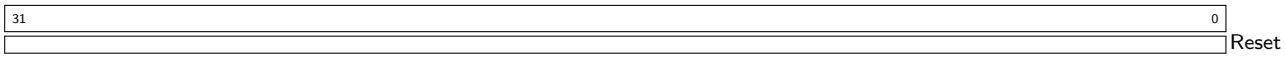
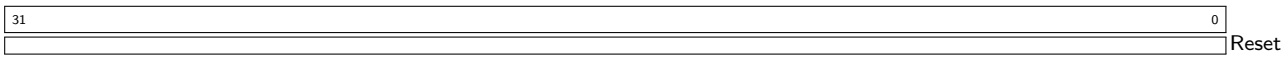
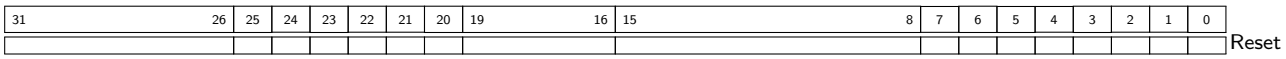

31
0
Reset


31
0
Reset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Reset

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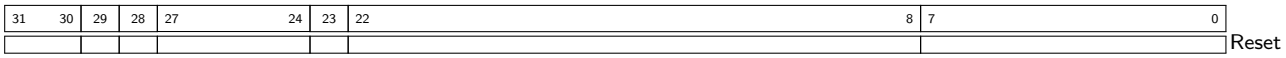
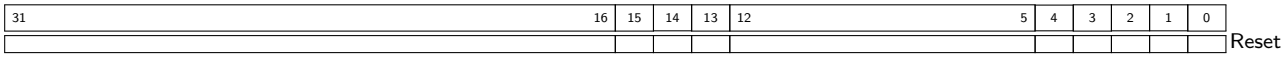

31 30
29
28
27 24
23
22 8
7 0
Reset


31
16
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14
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12
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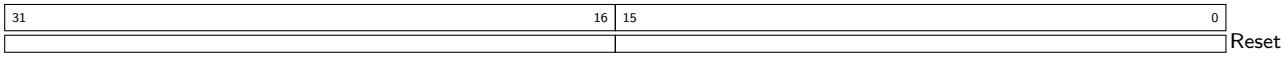
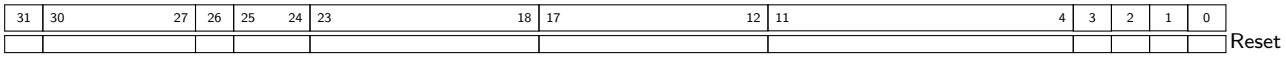
1
0
Reset


31
16
15
0
Reset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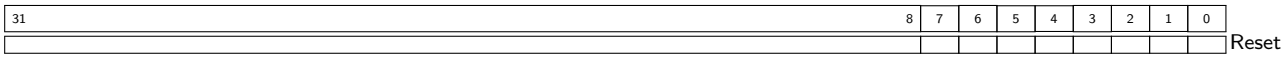
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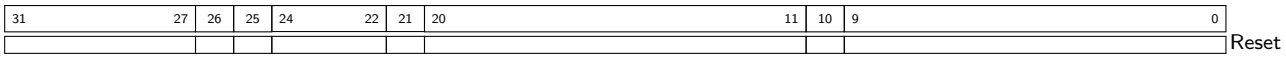
Reset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10
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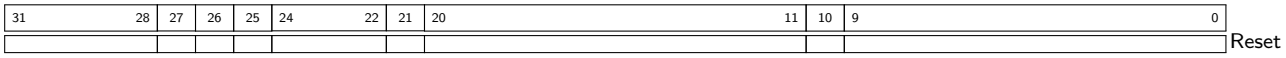
Reset


31 28
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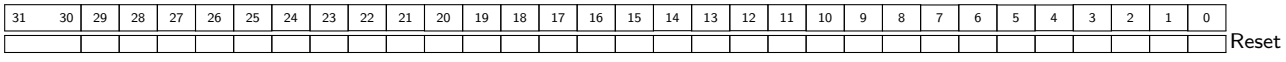
9 0
Reset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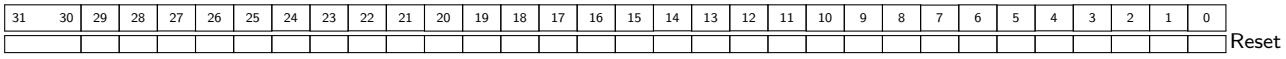
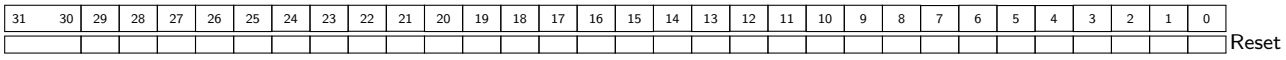
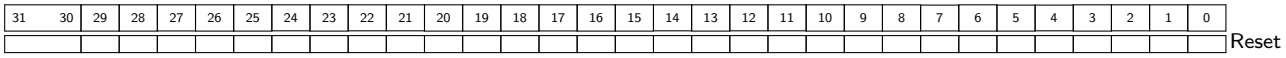
Reset


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Reset


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Reset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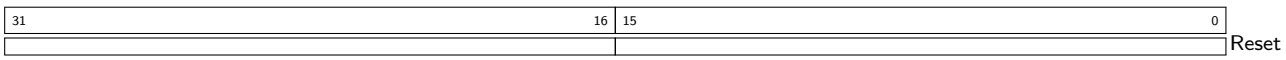
Reset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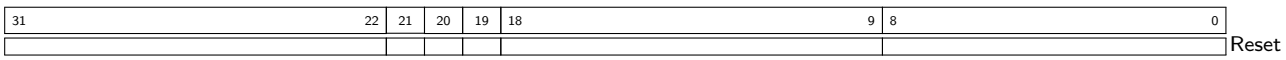
Reset


31
22
21
20
19
18
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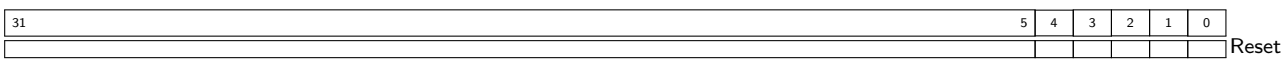
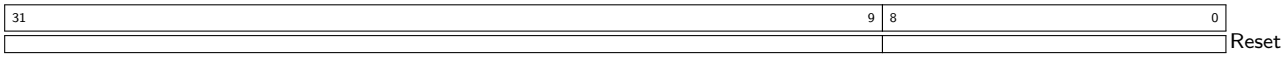
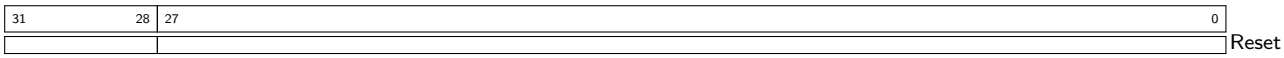
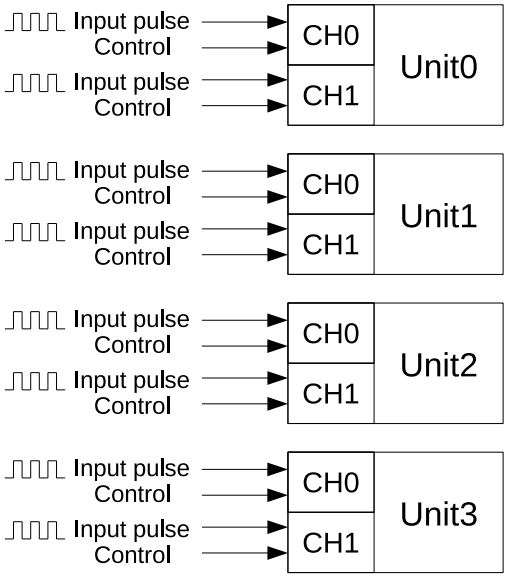
Reset


31
5
4
3
2
1
0
Reset


31
9
8
0
Reset


31
28
27
0
Reset


Input pulse
Control
Input pulse
Control
CH0
CH1
Unit0
Input pulse
Control
Input pulse
Control
CH0
CH1
Unit1
Input pulse
Control
Input pulse
Control
CH0
CH1
Unit2
Input pulse
Control
Input pulse
Control
CH0
CH1
Unit3

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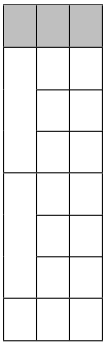

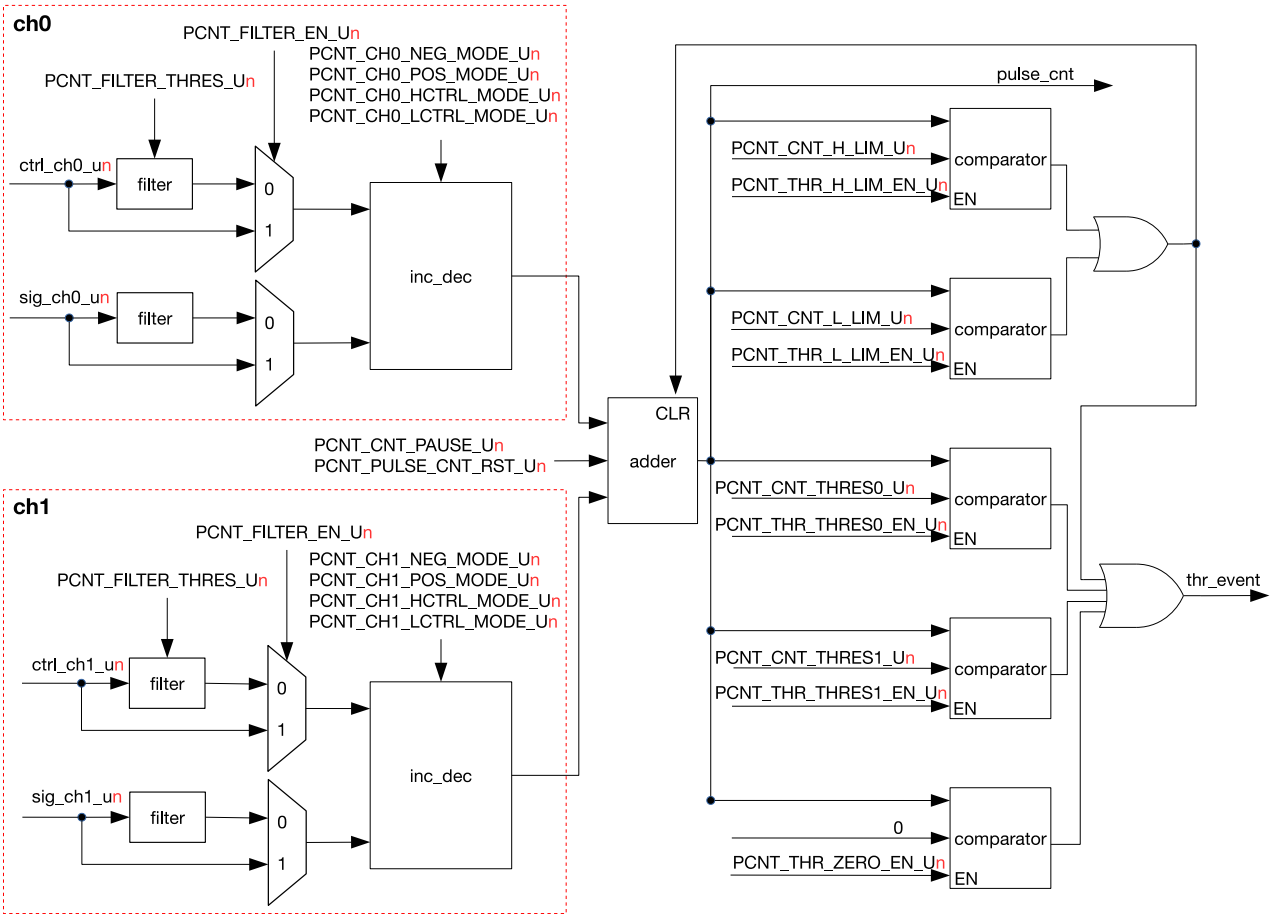
ch0
PCNT_FILTER_EN_Un
PCNT_CH0_NEG_MODE_Un
PCNT_CH0_POS_MODE_Un
PCNT_CH0_HCTRL_MODE_Un
PCNT_CH0_LCTRL_MODE_Un
PCNT_FILTER_THRES_Un
ctrl_ch0_un
filter
0
1
sig_ch0_un
filter
0
1
inc_dec
ch1
PCNT_FILTER_EN_Un
PCNT_CH1_NEG_MODE_Un
PCNT_CH1_POS_MODE_Un
PCNT_CH1_HCTRL_MODE_Un
PCNT_CH1_LCTRL_MODE_Un
PCNT_FILTER_THRES_Un
ctrl_ch1_un
filter
0
1
sig_ch1_un
filter
0
1
inc_dec
PCNT_CNT_PAUSE_Un
PCNT_PULSE_CNT_RST_Un
CLR
adder
pulse_cnt
PCNT_CNT_H_LIM_Un
PCNT_THR_H_LIM_EN_Un
comparator
EN
PCNT_CNT_L_LIM_Un
PCNT_THR_L_LIM_EN_Un
comparator
EN
PCNT_CNT_THRES0_Un
PCNT_THR_THRES0_EN_Un
comparator
EN
PCNT_CNT_THRES1_Un
PCNT_THR_THRES1_EN_Un
comparator
EN
0
PCNT_THR_ZERO_EN_Un
comparator
EN
thr_event

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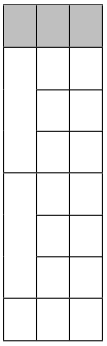

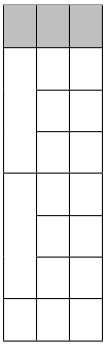

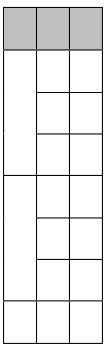

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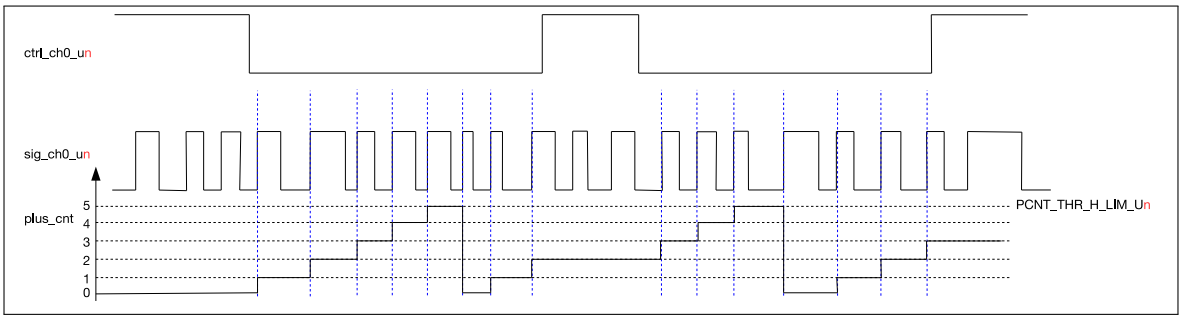
ctrl_ch0_un
sig_ch0_un
plus_cnt
5
4
3
2
1
0
PCNT_THR_H_LIM_Un

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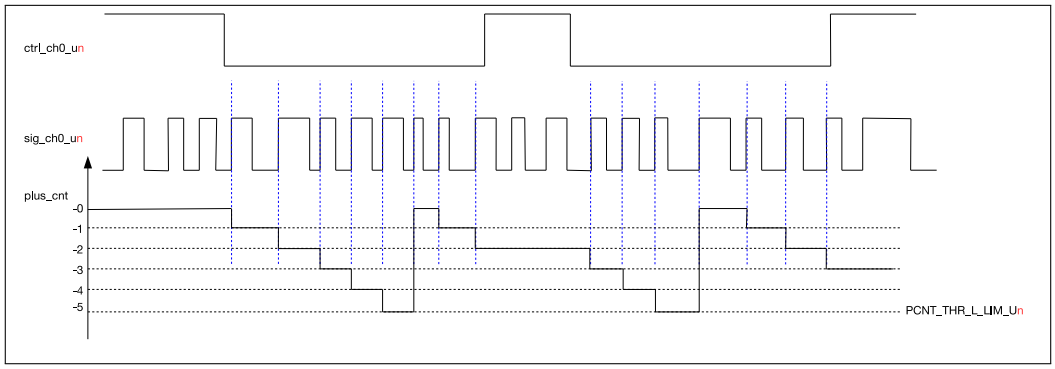
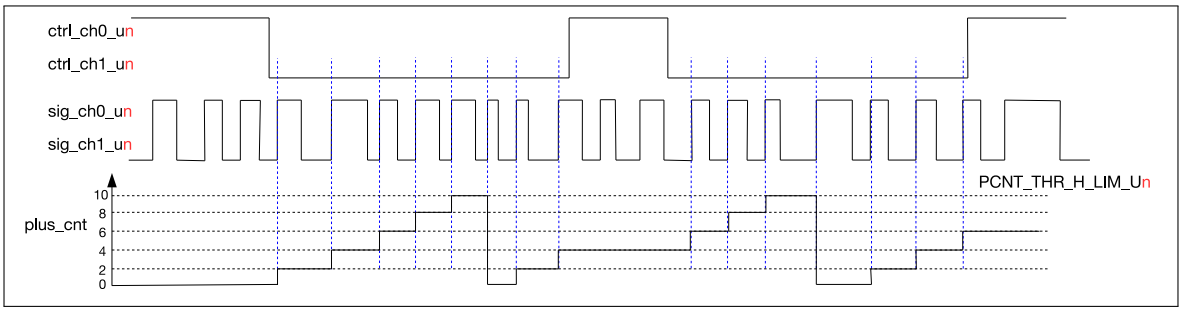

ctrl_ch0_un
sig_ch0_un
plus_cnt
-0
-1
-2
-3
-4
-5
PCNT_THR_L_LIM_Un

-
-


ctrl_ch0_un
ctrl_ch1_un
sig_ch0_un
sig_ch1_un
PCNT_THR_H_LIM_Un
plus_cnt
10
8
6
4
2
0

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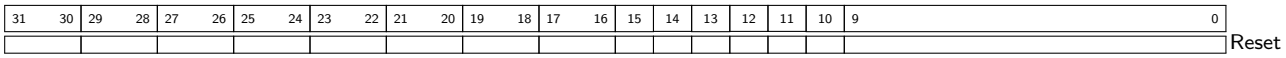
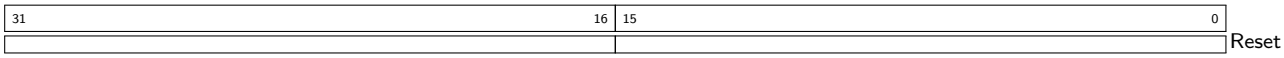
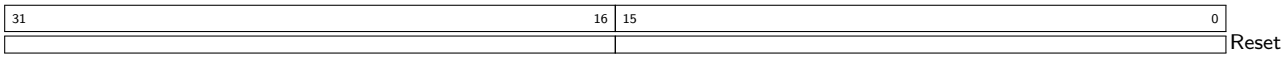
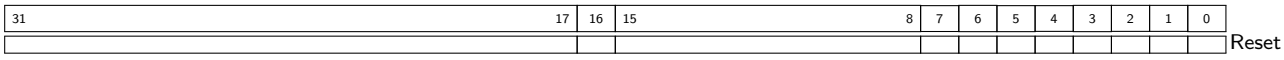
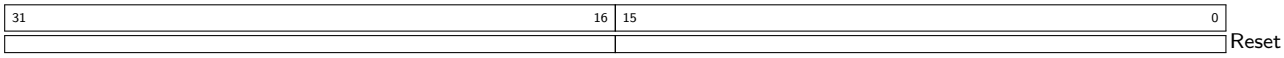
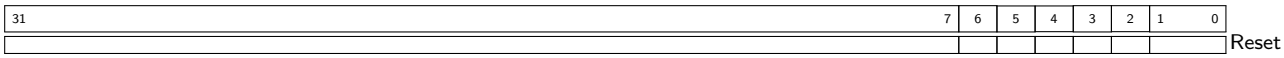

31 30
29 28
27 26
25 24
23 22
21 20
19 18
17 16
15
14
13
12
11
10
9 0
Reset

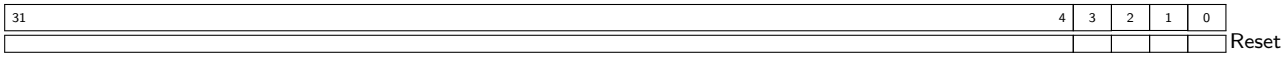

31
16
15
0
Reset

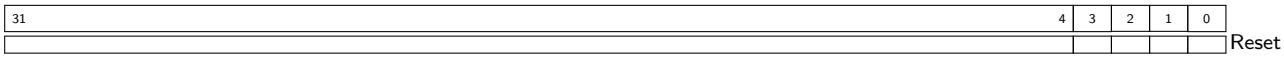

31
16
15
0
Reset

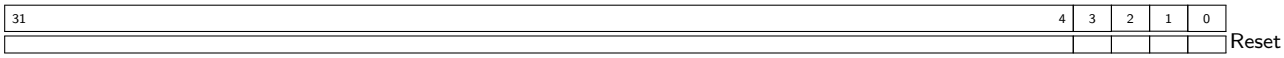

31
17
16
15
8
7
6
5
4
3
2
1
0
Reset

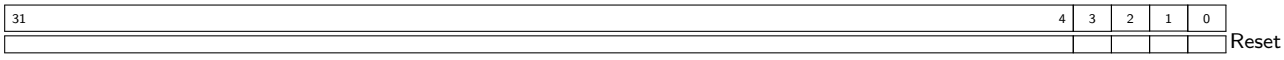

31
16
15
0
Reset

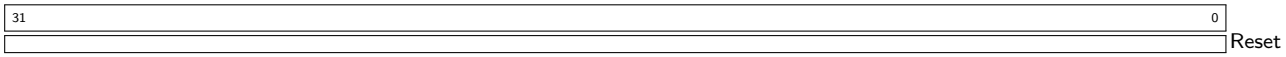

31
7
6
5
4
3
2
1
0
Reset


31
4
3
2
1
0
Reset


31
4
3
2
1
0
Reset


31
4
3
2
1
0
Reset


31
4
3
2
1
0
Reset


31
0
Reset

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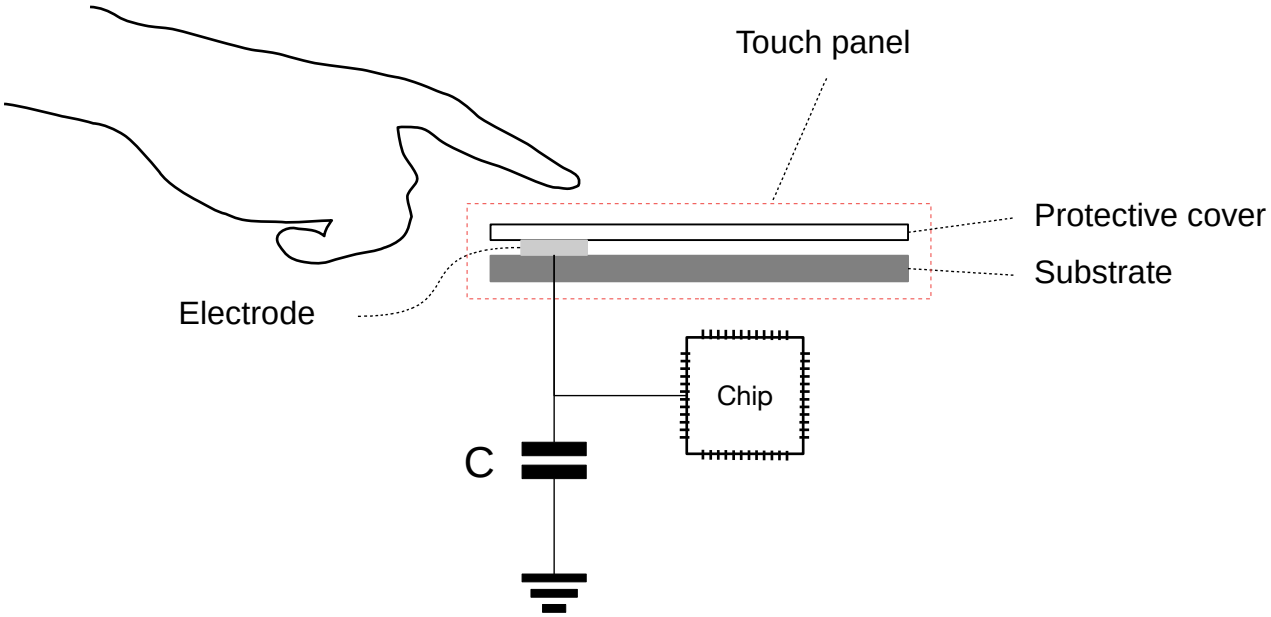
Touch panel
Protective cover
Substrate
Electrode
Chip
C

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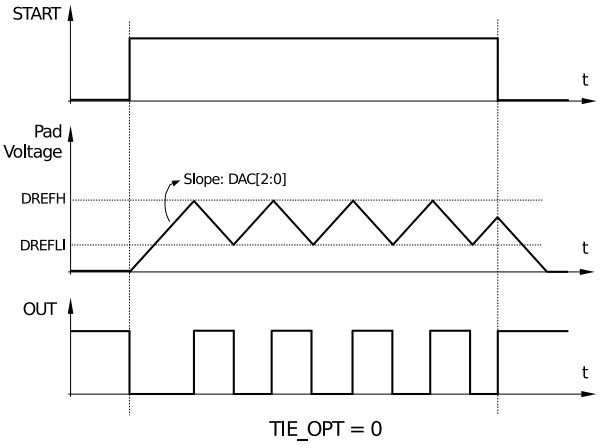
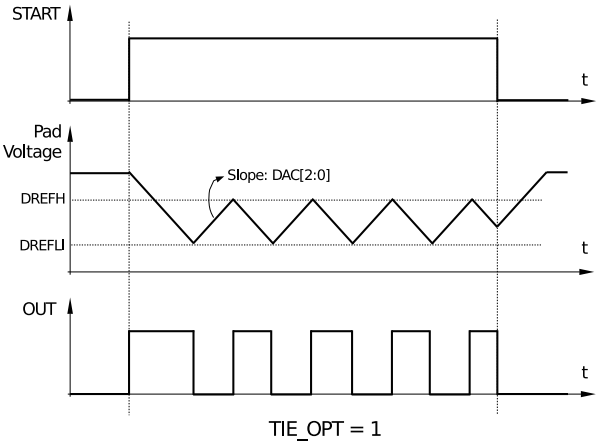
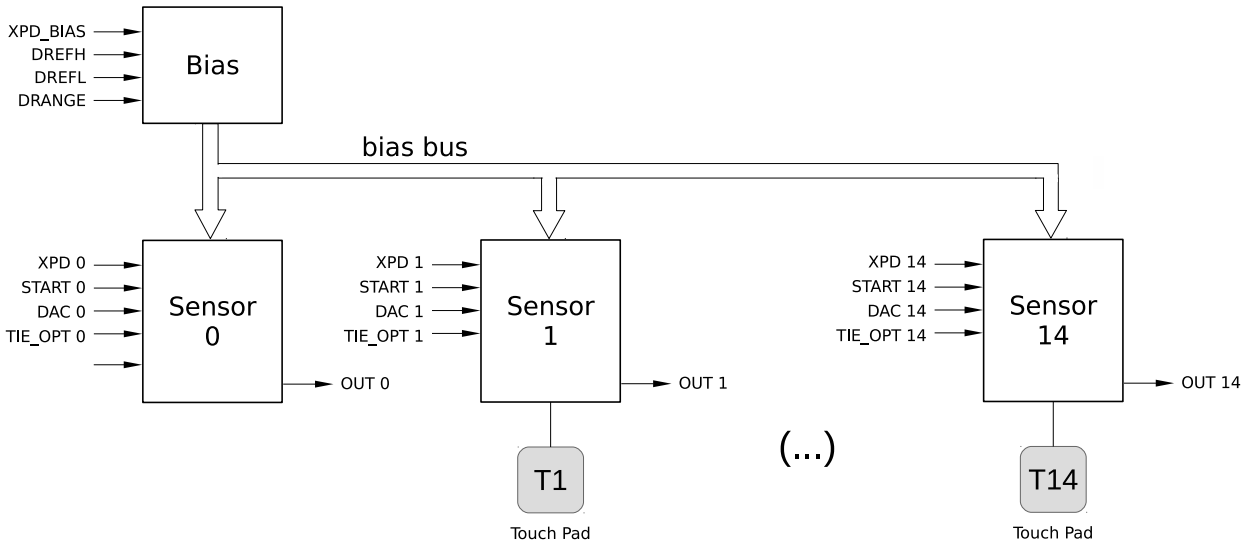


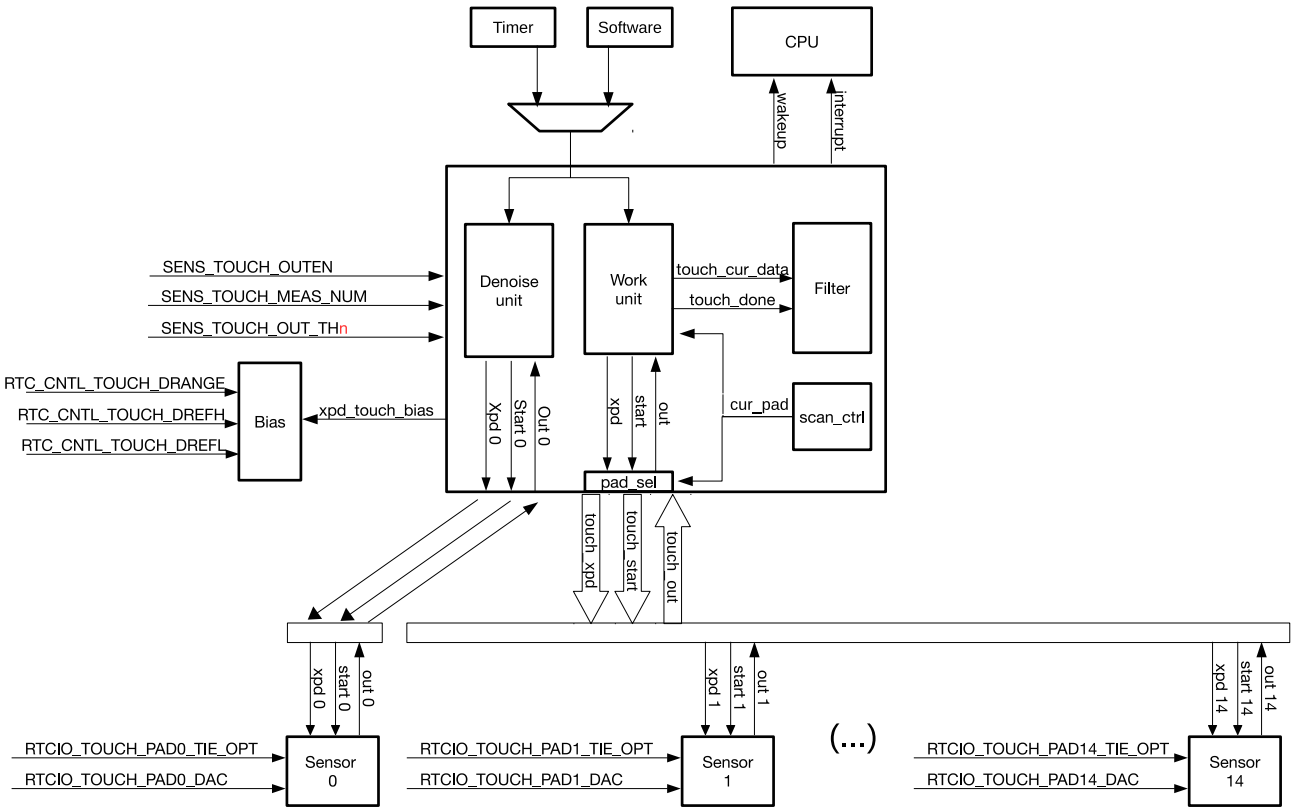
TIE_OPT = 0



TIE_OPT = 1


XPD_BIAS
DREFH
DREFL
DRANGE
Bias
bias bus
XPD 0
START 0
DAC 0
TIE_OPT 0
Sensor 0
OUT 0
XPD 1
START 1
DAC 1
TIE_OPT 1
Sensor 1
OUT 1
XPD 14
START 14
DAC 14
TIE_OPT 14
Sensor 14
OUT 14
(...)
T1
Touch Pad
T14
Touch Pad

-
-
-
-
-


Timer
Software
CPU
wakeup
interrupt
SENS_TOUCH_OUTEN
SENS_TOUCH_MEAS_NUM
SENS_TOUCH_OUT_THn
Denoise unit
Work unit
touch_cur_data
touch_done
Filter
RTC_CNTL_TOUCH_DRANGE
RTC_CNTL_TOUCH_DREFH
RTC_CNTL_TOUCH_DREFL
Bias
xpd_touch_bias
Xpd 0
Start 0
Out 0
xpd
start
out
cur_pad
scan_ctrl
pad_sel
touch_xpd
touch_start
touch_out
xpd 0
start 0
out 0
xpd 1
start 1
out 1
xpd 14
start 14
out 14
RTCIO_TOUCH_PAD0_TIE_OPT
RTCIO_TOUCH_PAD0_DAC
Sensor 0
RTCIO_TOUCH_PAD1_TIE_OPT
RTCIO_TOUCH_PAD1_DAC
Sensor 1
(...)
RTCIO_TOUCH_PAD14_TIE_OPT
RTCIO_TOUCH_PAD14_DAC
Sensor 14

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-
-
-

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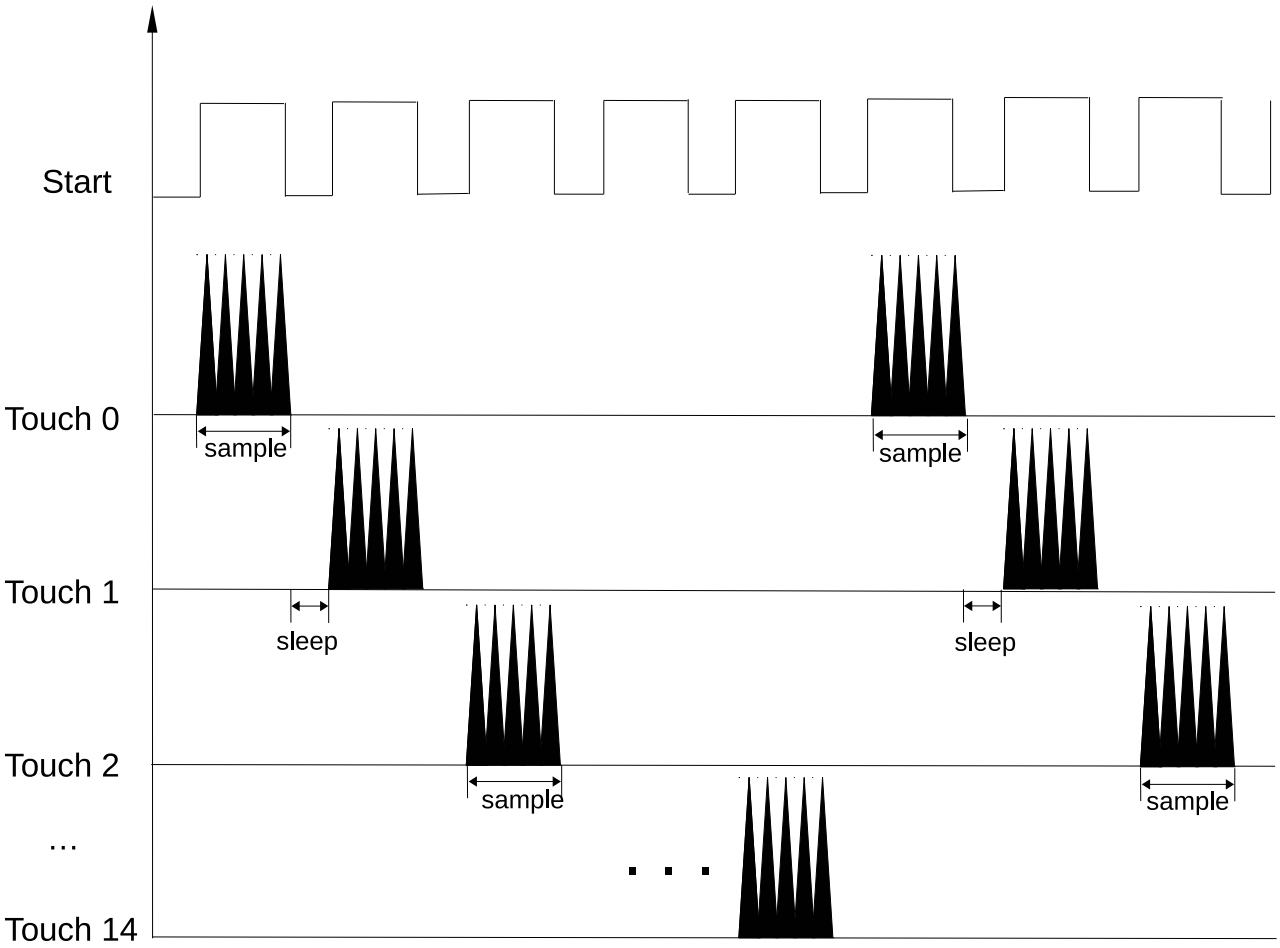
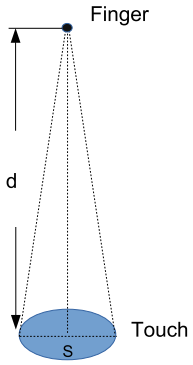
-


Start
Touch 0
sample
sample
Touch 1
sleep
sleep
Touch 2
sample
sample
…
Touch 14

-
-
-

-
-
-

- ^{2}
-



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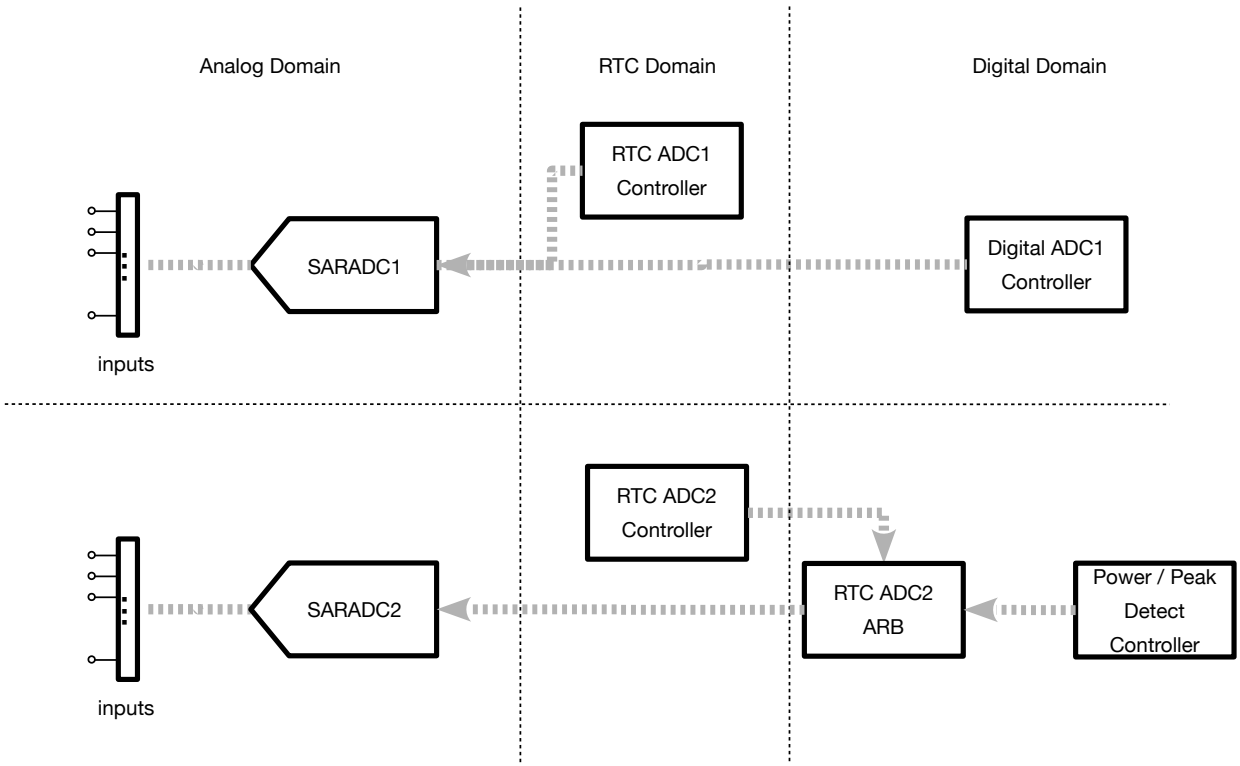
-


Analog Domain
RTC Domain
Digital Domain
RTC ADC1
Controller
SARADC1
Digital ADC1
Controller
inputs
RTC ADC2
Controller
SARADC2
RTC ADC2
ARB
Power / Peak
Detect
Controller
inputs

-
-
-

-
-
-
-
-
-

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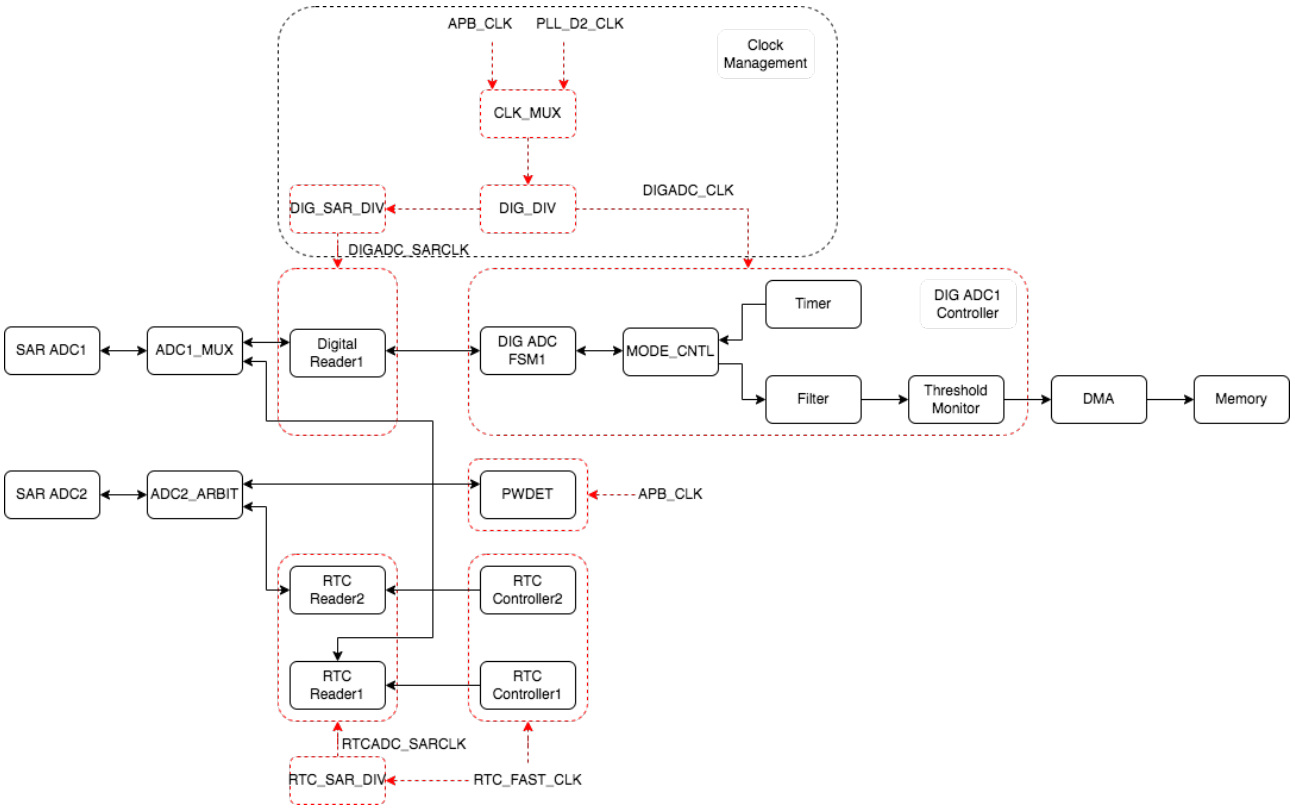
APB_CLK
PLL_D2_CLK
Clock Management
CLK_MUX
DIG_SAR_DIV
DIG_DIV
DIGADC_CLK
DIGADC_SARCLK
Timer
DIG ADC1 Controller
SAR ADC1
ADC1_MUX
Digital Reader1
DIG ADC FSM1
MODE_CNTL
Filter
Threshold Monitor
DMA
Memory
SAR ADC2
ADC2_ARBIT
PWDET
APB_CLK
RTC Reader2
RTC Controller2
RTC Reader1
RTC Controller1
RTCADC_SARCLK
RTC_SAR_DIV
RTC_FAST_CLK

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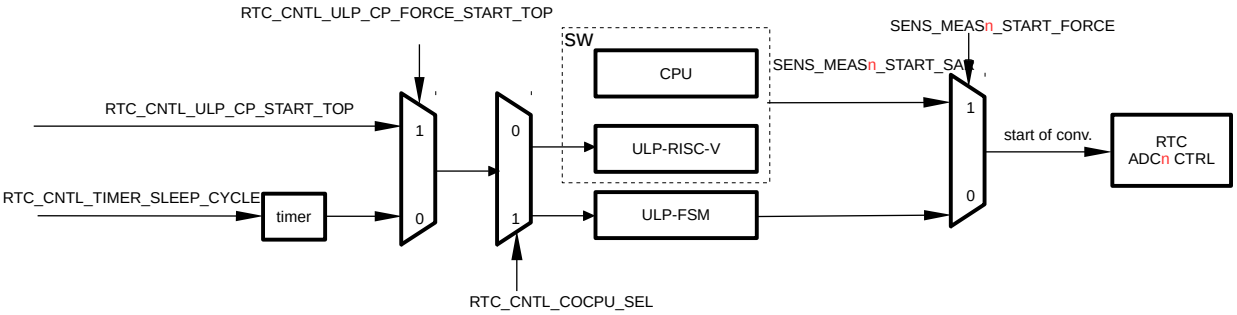
$V_{ref}V_{ref}V_{data}$

$$V_{data} = \frac{V_{ref}}{4095} \times data$$

V_{ref}


RTC_CNTL_ULP_CP_FORCE_START_TOP
SW
CPU
SENS_MEASn_START_FORCE
SENS_MEASn_START_SAR
RTC_CNTL_ULP_CP_START_TOP
1
0
ULP-RISC-V
start of conv.
RTC
ADCn CTRL
RTC_CNTL_TIMER_SLEEP_CYCLE
timer
ULP-FSM
RTC_CNTL_COCPU_SEL

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-
-
-
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-
-
-
-
-

-
-
-

-
-
-

31	24	23	18	17	12	11	6	5	0

31	24	23	18	17	12	11	6	5	0

31	24	23	18	17	12	11	6	5	0

31 24	23 18	17 12	11 6	5 0

5 2	1 0

-
-
-

5 2	1 0

5 2	1 0

-
-

32 17	15 13	12	11 0

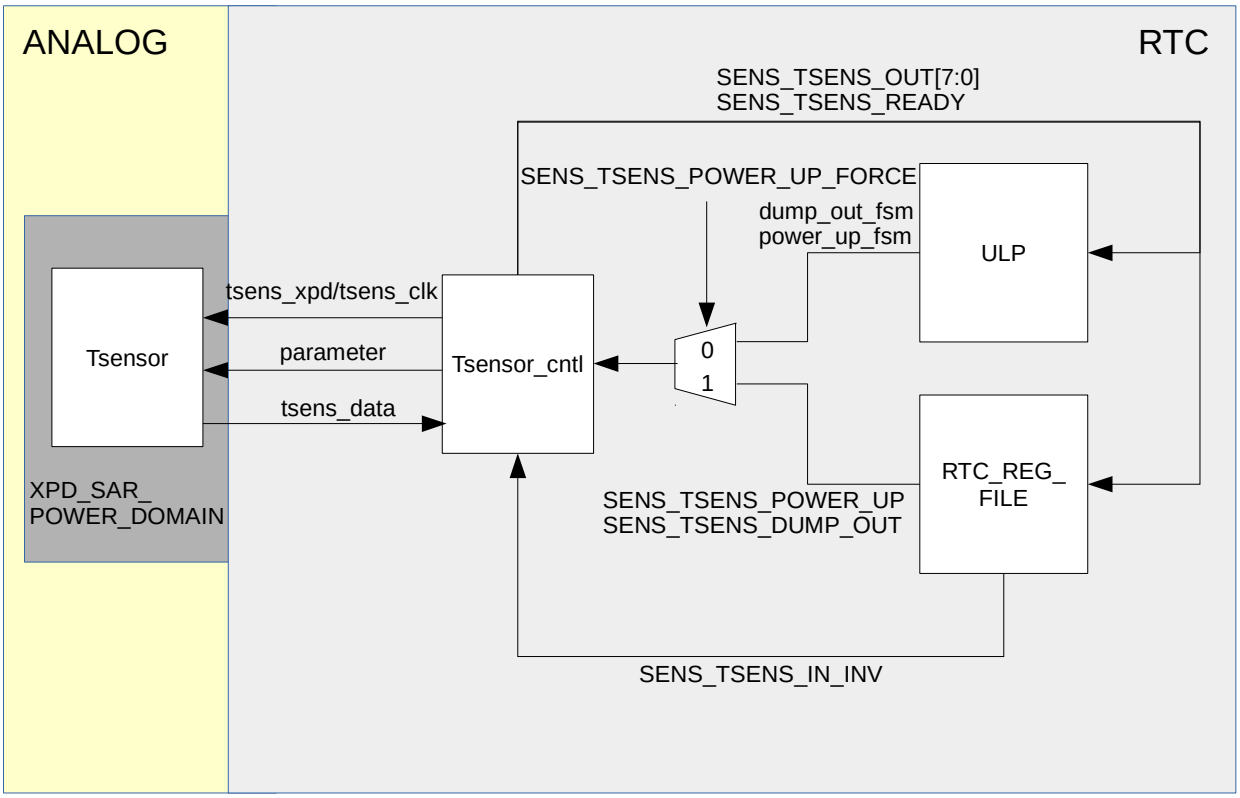
$$data_{cur} = \frac{(k-1)data_{prev}}{k} + \frac{data_{in}}{k} - 0.5$$

- $data_{cur}$
- $data_{in}$
- $data_{prev}$
- k

-
-

-
-
-
-

-
-
-
-
-
-
-
-


ANALOG
RTC
SENS_TSENS_OUT[7:0]
SENS_TSENS_READY
SENS_TSENS_POWER_UP_FORCE
dump_out_fsm
power_up_fsm
ULP
tsens_xpd/tsens_clk
parameter
tsens_data
Tsensor
Tsensor_cntl
0
1
RTC_REG_
FILE
XPD_SAR_
POWER_DOMAIN
SENS_TSENS_POWER_UP
SENS_TSENS_DUMP_OUT
SENS_TSENS_IN_INV

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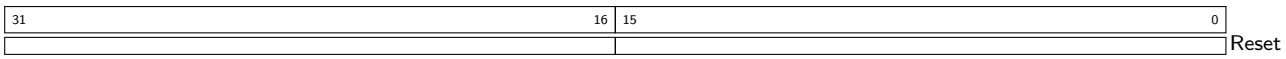
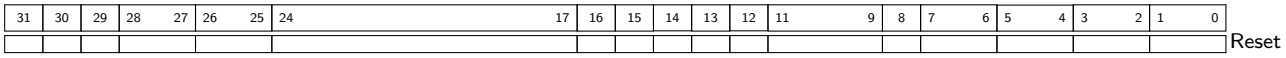
-
-

-
-
-


31
16
15
0
Reset


31
30
29
28
27
26
25
24
17
16
15
14
13
12
11
9
8
7
6
5
4
3
2
1
0
Reset

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-
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-
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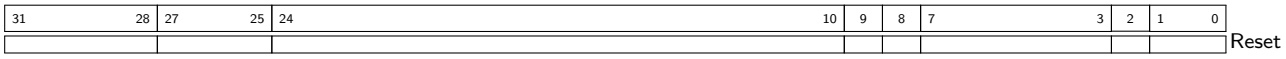
-


31 28
27 25
24 10
9
8
7 3
2
1 0
Reset

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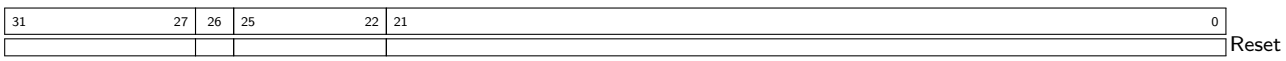
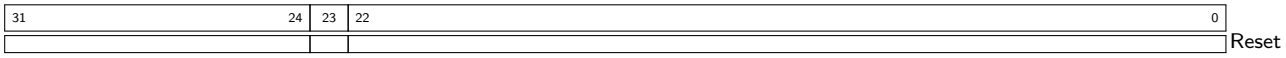
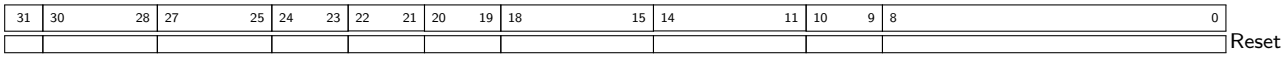
-
-
-


31 27
26
25 22
21 0
Reset


31
24
23
22
0
Reset


31
30
28
27
25
24
23
22
21
20
19
18
15
14
11
10
9
8
0
Reset

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-
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-
-
-
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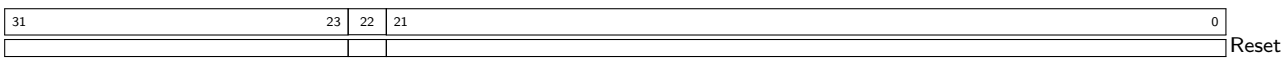
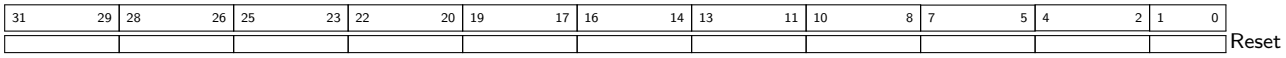
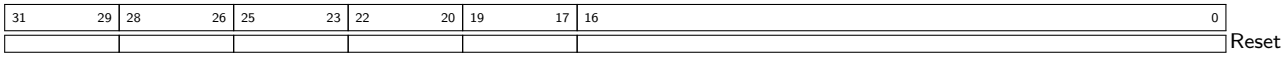
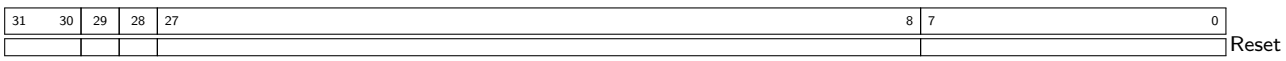
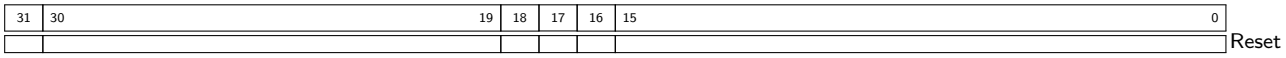
-

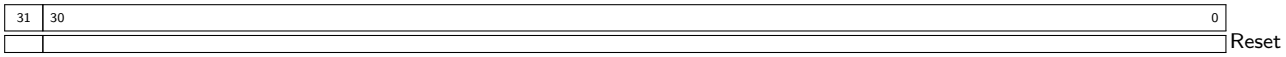

31
23
22
21
0
Reset

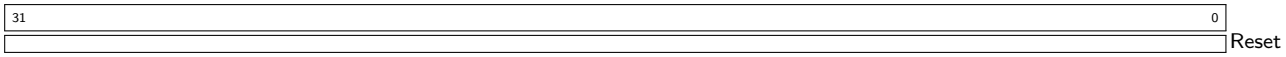

31 29
28 26
25 23
22 20
19 17
16 14
13 11
10 8
7 5
4 2
1 0
Reset

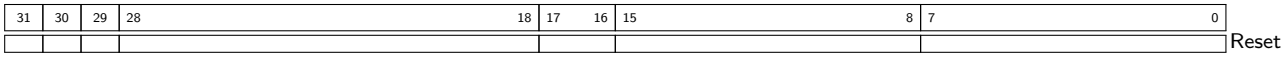

31 29
28 26
25 23
22 20
19 17
16 0
Reset

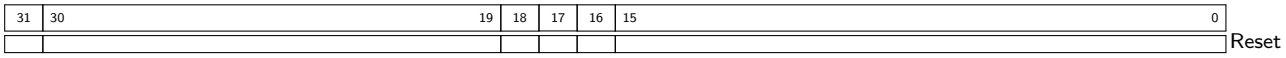

31 30
29
28
27 8
7 0
Reset

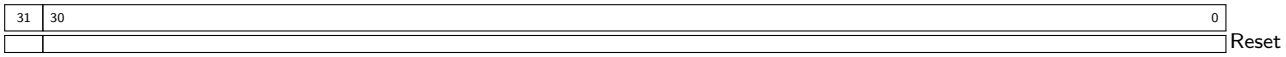

31
30
19
18
17
16
15
0
Reset

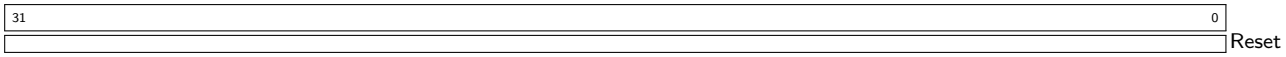

31
30
0
Reset

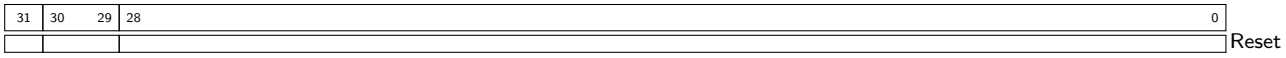

31
0
Reset

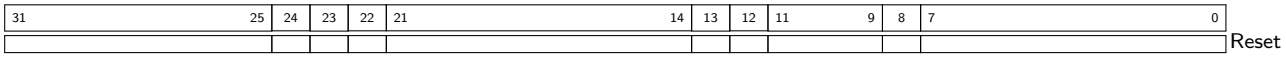

31
30
29
28
18
17
16
15
8
7
0
Reset

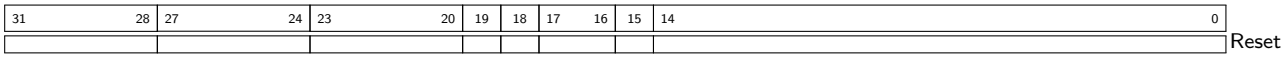

31
30
19
18
17
16
15
0
Reset


31
30
0
Reset


31
0
Reset


31
30
29
28
0
Reset


31
25
24
23
22
21
14
13
12
11
9
8
7
0
Reset


31
28
27
24
23
20
19
18
17
16
15
14
0
Reset

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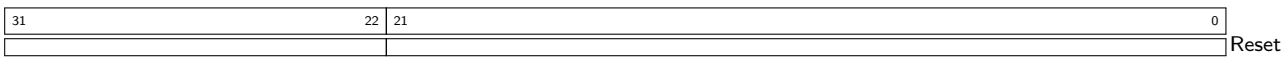
31
22
21
0
Reset

31	22	21	0	
				Reset

31	22	21	0	
				Reset

31	22	21	0	
				Reset

31	22	21	0	
				Reset

31	22	21	0	
				Reset

31	22	21	0	
				Reset

31	22	21	0	
				Reset

31	22	21	0	
				Reset

31	22	21	0	
				Reset

31	22	21	0	
				Reset

31	22	21	0	
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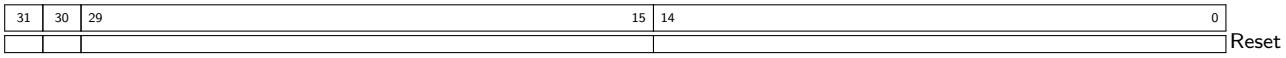
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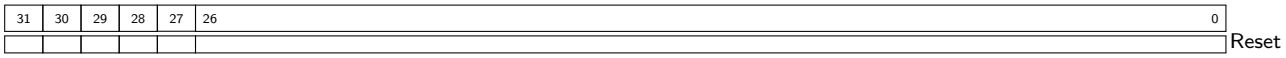
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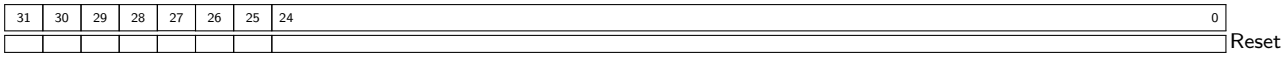
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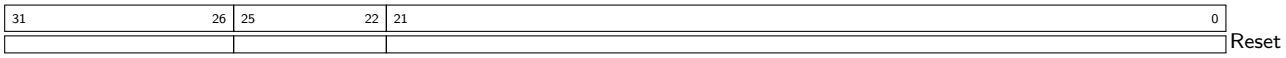
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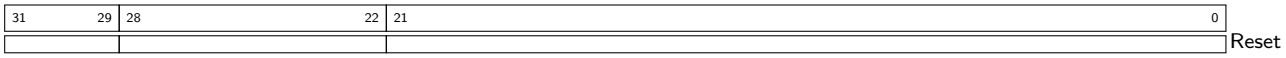
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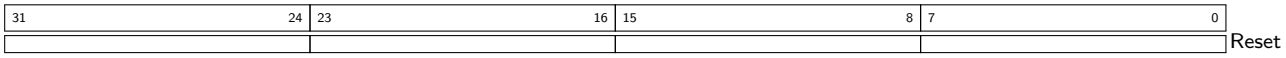
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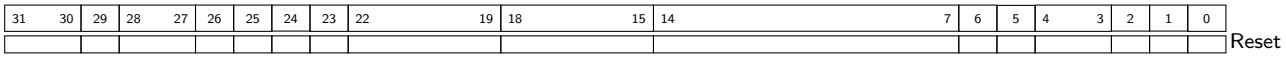
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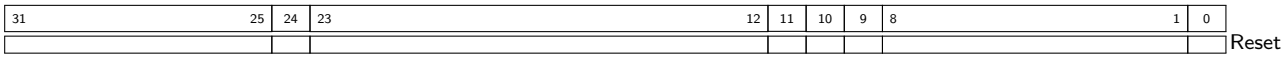
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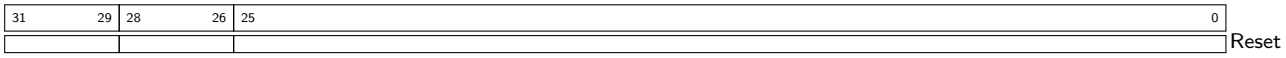
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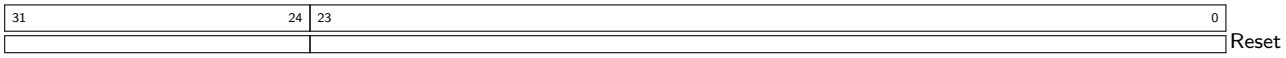
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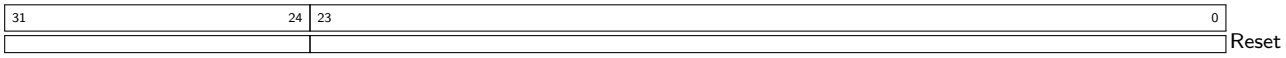
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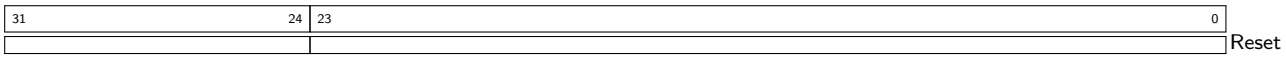
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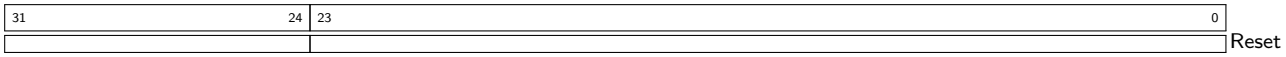
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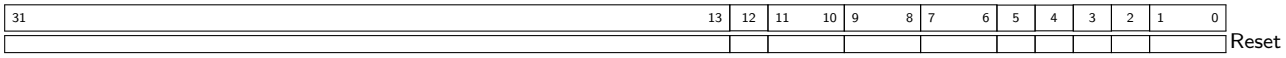
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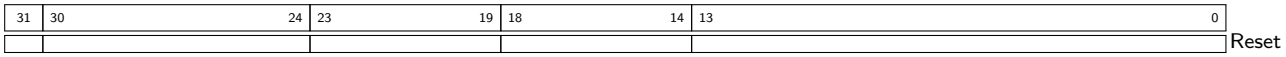
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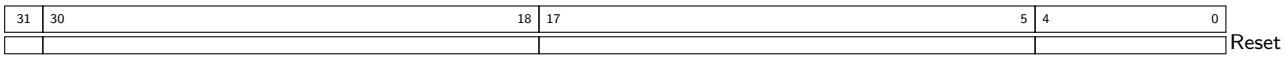
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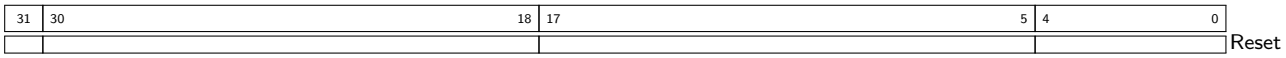
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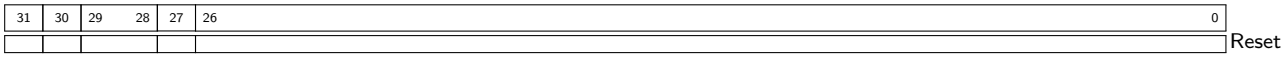
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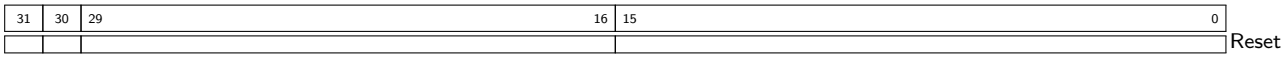
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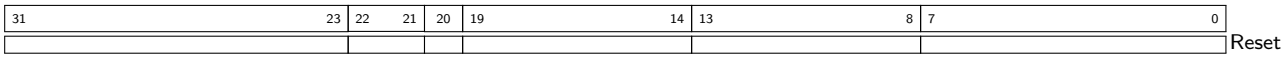
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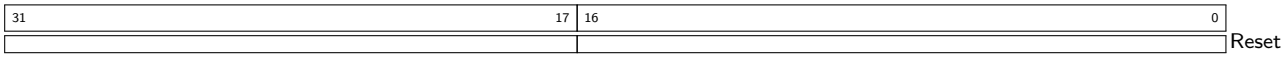
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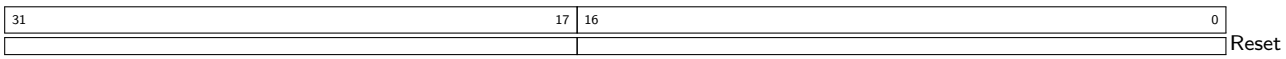
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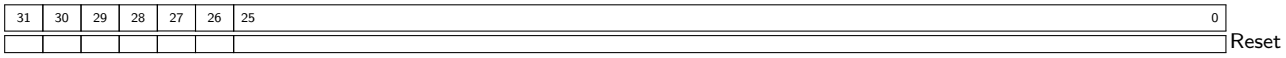
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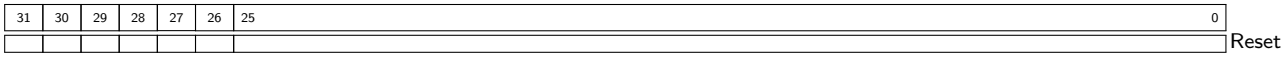
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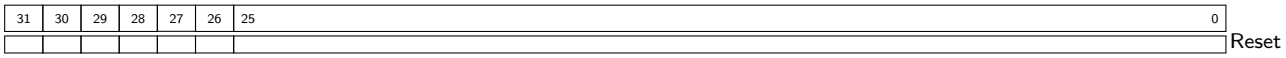
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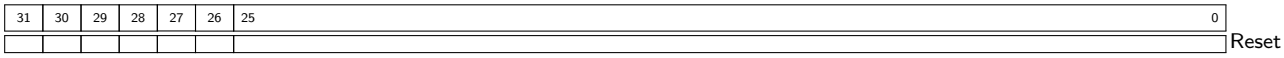
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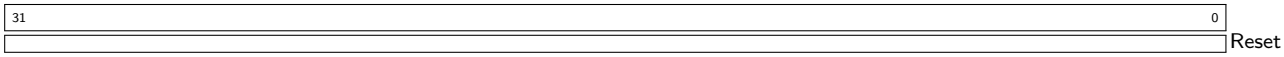
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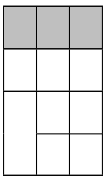

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